LOW POWER VLSI DESIGN

Course Code: 13EC2211 **L P C**
4 0 3

Pre requisites: EDC, DICA, VLSI Design.

Course Educational Objectives:

1. This course addresses a profound analysis on the development of the CMOS & Bi-CMOS digital circuits for a low voltage low power environment
2. To study the concepts of device behavior and modeling
3. To study the concepts of low voltage, low power logic circuits.

Course Outcomes:

1. Capability to recognize advanced issues in VLSI systems, specific to the deep-submicron silicon technologies.
2. Students able to understand deep submicron CMOS technology and digital CMOS design styles.
3. To design chips used for battery-powered systems and high-performance circuits

UNIT- I
INTRODUCTION TO LOW POWER DESIGN:
Introduction, Low Power design- an overview, low power design limitations: power supply voltage, threshold voltage, scaling, interconnect wires, Silicon-on-Insulator (SOI) From Devices to Circuits.

UNIT-II
MOS/BI-CMOS PROCESS TECHNOLOGY AND INTEGRATION:
The Realization of Bi-CMOS processes, Bi-CMOS manufacturing and Integration Considerations, Isolation in Bi-CMOS, Deep submicron processes, Future trends and directions of CMOS/Bi-CMOS processes.

UNIT-III
DEVICE BEHAVIOR AND MODELING:
The MOS (FET) Transistor, The Bipolar (Junction) transistor, MOSFET SPICE models, Advanced, Bipolar Spice models, MOSFET

in Hybrid Mode Environment-Surface p-Channel for Sub-Half-Micron Devices, Device Fabrication, Model Parameters Extraction, Sub-Half-Micron D.C. Model Formulation.

UNIT-IV

CONVENTIONAL CMOS AND BI-CMOS LOGIC GATES:

Conventional CMOS Logic Gates, Conventional Bi-CMOS Logic Gate, Bi-CMOS Circuits Utilizing Lateral pnp BJTs in pMOS structures, Performance evaluation and Comparison.

UNIT-V

LOW- VOLTAGE, LOW POWER LOGIC CIRCUITS:

Merged Bi-CMOS digital circuits, Full-Swing Multidrain/ Multicollector Complementary Bi-CMOS Buffers, Quasi-Complementary Bi-CMOS Digital Circuits, Full-Swing Bi-CMOS/Bi-NMOS Digital circuits employing Schottky Diodes, Feedback-Type Bi-CMOS Digital Circuits, High-Beta Bi-CMOS Digital Circuits, Transiently Saturated Full-Swing Bi-CMOS Digital Circuits, Bootstrapped-type Bi-CMOS Digital circuits,ESD-free Bi-CMOS Digital circuit -circuit operation and comparative Evaluation.

Evolution of Latches and Flip-Flops, Quality Measures for Latches and Flip-Flops, Design perspective.

TEXT BOOK:

[1] KiatSeng Yeo, Samir S. Rofail, Wang-Ling Goh, "*CMOS/Bi CMOS ULSI Low Voltage Low Power*", Pearson Education Asia 1st Indian reprint, 2002.

REFERENCE BOOKS:

[1] J.Rabaey, "*Digital Integrated Circuits*", PH. N.J 1996, 2nd Edition.

[2] Sung-mokang and yusufleblebici, "*CMOS Digital ICs*", TMH, 3rd edition, 2003.

[3] Parhi, "*VLSI DSP Systems*", John Wiley & sons, 2003 Reprint.

[4] IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.