HDL PROGRAMMING LABORATORY

Course Code: 13EC2208 **L P C**
0 3 2

Pre requisites: VHDL, Verilog, Switching Theory and Logic Design.

Course Objective:

1. To model a digital system using VHDL/Verilog Hardware Description Languages.
2. Implementation of digital circuits using programmable devices.

Course outcomes:

1. Students will be able to design, simulate and synthesize combinational and sequential circuits using VHDL and Verilog Hardware Description Languages.
2. Students will get hands on experience on XILINX/CADENCE Platforms.
3. Students will get hands on experience on FPGA/CPLD.

LIST OF EXPERIMENTS

1. 16 X 1 MULTIPLEXER
2. 4-Bit ALU
3. 8-Bit UP/DOWN COUNTER
4. 32 X 8 ROM
5. SEQUENCE DETECTOR 101(using Mealy Machine)
6. SEQUENCE DETECTOR 1011(using Moore Machine)
7. DECODERS
8. 8-Bit SHIFT REGISTER
9. BCD ADDER
10. PARITY CHECKER
11. SEQUENCE GENERATOR
12. 8-BIT COMPARATOR
13. BARREL SHIFTER
14. UNIVERSAL SHIFT REGISTER

STEPS FOLLOWED DURING EXPERIMENTATION

1. Digital Circuits Description using Verilog and VHDL
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits.
5. Implementation of Designed Digital Circuits using FPGA and CPLD devices.