ELECTRONIC DESIGN AUTOMATION TOOLS
(ELECTIVE – II)

Course Code: 13EC2213 **L P C**
4 0 3

Pre requisites: PSPICE, VERILOG, VHDL

Course Educational Objectives:

1. This Course gives an idea about the tools and techniques for integrated circuit design

Course Outcomes:

1. This course deals with Functional design and verification, Front-end, Back-end IC design flow and tools, Mixed signal design flow for integrated circuit design.
2. Capability in Microelectronics design and Implementation using Electronic Design Automation (EDA) tools.

UNIT-I
SIMULATION USING HDLS:
Simulation-Types of Simulation, Logic Systems, Working of Logic Simulation, Cell Models, Delay Models, State Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation.

UNIT-II
SYNTHESIS USING HDLS:
Verilog and Logic Synthesis, VHDL and Logic Synthesis, Memory Synthesis, FSM Synthesis, Memory Synthesis, Performance-Driven Synthesis.
CAD Tools for Simulation and Synthesis: Modelsim and Leonardo Spectrum

UNIT-III
CIRCUIT DESIGN AND SIMULATION USING PSPICE:
Pspice Models For Transistors, A/D & D/A Sample And Hold Circuits etc., and Digital System Building Blocks, Design and Analysis of Analog and Digital Circuits Using PSPICE.

UNIT-IV

AN OVERVIEW OF MIXED SIGNAL VLSI DESIGN:

Fundamentals Of Analog And Digital Simulation, Mixed Signal Simulator Configurations, Understanding Modeling, Integration To CAD Environments.

UNIT-V

TOOLS FOR PCB DESIGN AND LAYOUT:

An Overview of High Speed PCB Design, Design Entry, Simulation and Layout Tools for PCB, Introduction to Orcad PCB Design Tools.

TEXTBOOKS:

[1] J.Bhaskar, "*A Verilog Primer*", BSP, 2003.

[2] J.Bhaskar, "*A Verilog HDL Synthesis*", BSP, 2003.

[3] M.H.RASHID, "*SPICE FOR Circuits and Electronics Using PSPICE*", (2/E) (1992) Prentice Hall.

REFERENCE BOOKS:

[1] ORCAD: Technical Reference Manual, Orcad, USA.

[2] SABER, "*Technical Reference Manual*", Analogy Nic, USA.

[3] M.J.S.SMITH, "*Application-Specific Integrated Circuits*", (1997). Addison Wesley.

[4] J.Bhaskar, "*A VHDL Synthesis Primer*", BSP, 2003.