CPLD AND FPGA ARCHITECTURE AND APPLICATIONS (ELECTIVE – I)

Course Code: 13EC2205 **L P C**
4 0 3

Pre requisites: Programmable logic devices, combinational and sequential logic circuit design.

Course Educational Objectives:

1. Familiarization of various complex programmable Logic devices of different families.
2. To study Field programmable gate arrays and realization techniques.
3. To study different case studies using one hot design methods.

Course Outcomes:

1. Able to gain the knowledge about PLDs, FPGA Design & architectures.
2. Students should be able to understand different types of arrays.
3. FSM and different FSM techniques like petrinets, and different case studies.

UNIT-I

PROGRAMMABLE LOGIC DEVICES:

Complex Programmable Logic Devices (CPLD):

ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic – 10000 series CPLD, AMD's – CPLD (Mach 1 to 5); Cypres FLASH 370 Device Technology, Lattice LSI's Architectures – 3000 Series – Speed Performance and in system programmability.

Field Programmable Gate Arrays (FPGA)

Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs

UNIT-II

FPGA/CPLD ARCHITECTURES:

Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1, 2, 3 and their speed performance

UNIT-III

FINITE STATE MACHINES (FSM):

Top Down Design – State Transition Table, state assignments for FPGAs. Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL.

Alternative realization for state machine chart using microprogramming. Linked state machines. One – Hot state machine, Petrinets for state machines – basic concepts, properties, extendedpetrinets for parallel controllers. FiniteStateMachine – Case Study, Meta Stability, Synchronization.

UNIT-IV

FSM ARCHITECTURES:

Architectures centered around non-registered PLDs. State machine designs centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. Application of One – Hot method.

UNIT-V

SYSTEM LEVEL DESIGN:

Controller, data path and functional partitions, Parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

TEXT BOOKS:

[1] P.K.Chan& S. Mourad, "*Digital Design Using Field Programmable Gate Array*", prentice Hall (Pte), 1994.

[2] S.Brown, R.Francis, J.Rose, Z.Vransic, "*Field Programmable Gate Array*", Kluwer Publications, 1992.

REFERENCE BOOKS:

[1] J. Old Field, R.Dorf, "*Field Programmable Gate Arrays*", John Wiley & Sons, New York, 1995.

[2] S.Trimberger, Edr. "*Field Programmable Gate Array Technology*", Kluwer Academic Publications, 1994.

[3] Bob Zeidman, "*Designing with FPGAs &CPLDs*",CMPBooks, 2002.