VLSI TECHNOLOGY & DESIGN
(ELECTIVE – I)

Course Code: 13EC2202

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Pre requisites: Electronics Devices and Circuits, Switching Theory and Logic Design.

Course Educational Objectives:

1. This course provides an introduction to the design, analysis and layout of VLSI Circuits.

Course Outcomes:

1. Students understand the basic transistor theory, electrical properties of MOS circuits.
2. Students will be able to apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
3. Students will be able to understand different CMOS technology issues: Deep submicron design, clocking, power optimization, CAD tools and algorithms and design methodology.

UNIT-I
BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICMOS CIRCUITS:

Review of Microelectronics: (MOS, CMOS, Bi CMOS) Technology trends and projections, Ids-Vds relationships, Threshold voltage V_t, G_m, G_{ds}andW_o, Pass Transistor, MOS, CMOS &Bi-CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT-II
LAYOUT DESIGN AND TOOLS:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Diagrams for NMOS and CMOS Inverters and Gates, Layout Design tools.

UNIT-III
LOGIC GATES &COMBINATIONAL LOGIC NETWORKS:

Static complementary gates, switch logic, Alternative gate circuits, low

power gates, Resistive and Inductive interconnect delays. Layouts, Simulation, Network delay, interconnect design, power optimization, Switch logic networks, Gate and Network testing.

UNIT-IV

SEQUENTIAL SYSTEMS:

Memory cells and Arrays, clocking disciplines, Design, power optimization, Design validation and testing.

UNIT-V

FLOOR PLANNING &CHIP DESIGN:

Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing. Introduction to cad systems (algorithms) and chip design - Layout Synthesis and Analysis, Scheduling and binding, Hardware/Software Co-design, chip design methodologies- A simple Design example.

TEXTBOOKS:

[1] Kamran Eshraghian, EshraghianDougles and A.Pucknell, "*Essentials of VLSI circuits and systems*", 3rd Edition, PHI, 2005.

[2] Wayne Wolf, "*Modern VLSI Design*", Pearson Education, 3rd Edition, 2008.

REFERENCES:

[1] Weste and Eshraghian, "*Principles of CMOS VLSI Design*", Pearson Education, 3rd Edition, 1999.

[2] Fabricius, "*Introduction to VLSI Design*", MGH International Edition, 1990.

[3] Baker and Li Boyce, "*CMOS Circuit Design, Layout and Simulation*", PHI, 2004.