DSP PROCESSORS & ARCHITECTURE

Course Code: 13EC2113

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Pre requisites: Knowledge of signals and systems, convolution methods, digital signal processing concepts.

Course Educational Objectives:

1. To impart the knowledge of basic DSP filters and number systems.
2. To introduceconcepts of digital signal processing techniques, implementation of DSP & FFT algorithms by programming the DSP TMS320C54XX PROCESSOR and also to learn about interfacing of serial & parallel communication peripherals.

Course Outcomes:

1. Student has the knowledge & concepts of digital signal processing techniques, basic building blocks,implementation of DSP & FFT algorithms.
2. Capability for programming the DSP TMS320C54XX PROCESSOR and decimation interpolation filters, adaptive filters
3. Interface serial & parallel communication devices like CODEC to the processor.

UNIT-I

INTRODUCTION:

Introduction, Digital signal-processing system, sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation,Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors.

UNIT-II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT-III

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-IV

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS:

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT-V

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

[1] Avtar Singh and S. Srinivasan, "*Digital Signal Processing*" Thomson Publications, 2004.

[2] Lapsley et al., "*DSP Processor Fundamentals, Architectures & Features*", S. Chand & Co, 2000.

REFERENCES

[1] B. VenkataRamani and M. Bhaskar, "*Digital Signal Processors, Architecture, Programming and Applications*" TMH, 2004.

[2] Jonatham Stein, "*Digital Signal Processing*", John Wiley, 2000.