ACADEMIC REGULATIONS

COURSE STRUCTURE AND SYLLABI

FOR

M.TECH.
COMMUNICATIONS & SIGNAL PROCESSING
(Electronics and Communications Engineering)
2012-2013

GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING
(AUTONOMOUS)
ACCREDITED BY **NAAC** WITH **A** GRADE WITH A **CGPA** OF **3.47/4.00**
AFFILIATED TO JNTU KAKINADA
MADHURAWADA, VISAKHAPATNAM 530048

Vision

To evolve into and sustain as a Centre of Excellence in Technological Education and Research with a holistic approach.

Mission

To produce high quality engineering graduates with the requisite theoretical and practical knowledge and social awareness to be able to contribute effectively to the progress of the society through their chosen field of endeavor.

To undertake Research & Development, and extension activities in the fields of Science and Engineering in areas of relevance for immediate application as well as for strengthening or establishing fundamental knowledge.

F O R E W O R D

It is three years since the G.V.P College of Engineering has become Autonomous with the appreciation and support of erstwhile JNTU and the fast growing new JNTU-K. The college is progressing well with its programmes and procedures drawing more and more accolades from its sister autonomous colleges and higher authorities. The student community, also could adjust well to the new system without any acrimony.

The College is enriched with the experience of running the Post-graduate programmes under Autonomous stream. It is a moment of pride and achievement that the first Autonomous batch of M.Tech in some branches left the college to the satisfaction of all concerned including firms visited the campus for placements.

Another larger than canvas picture is foreseen for the programmes wherein the college is getting the funds through TEQIP – II for up-scaling the PG education and research under sub- component 1.2. In this connection two new PG Programmes have been introduced in Mechanical, Electrical Engineering.

New set of Boards of Studies, Academic council and Governing Body has further strengthened our hands by endorsing the practices and suggested recommendations.
The encouragement given by the affiliating JNTU-K has left no task insurmountable.

Principal

MEMBERS ON THE BOARD OF STUDIES
IN
ELECTRONICS AND COMMUNICATIONS ENGINEERING

- Head of the Department.

- Dr. B. Prabhakara Rao, Professor, Dept. of ECE & Director of Foreign Affairs, JNTU-K, Kakinada.
- Dr. R.V.S. Satyanarayana, Professor, Department of E.C.E., S.V.U. College of Engg., Tirupati.
- Sri Abraham Verghese, Scientist 'F', Additional Director, NSTL, Visakhapatnam.
- Dr. Namburi Nageswara Rao, Principal, SITAM, Vizianagaram.
- Dr. K. Rajarajeswari, Professor and Chairman, Board of Studies,Dept. of ECE, Andhra University, Visakhapatnam.
- Sri P. Nagaraju, General Manager, BSNL, Visakhapatnam.
- Sri M. Bhuvan Kiran, Management Trainee, Vizag Steel Plant, Visakhapatnam.

All faculty of the department.

ACADEMIC REGULATIONS

(Effective for the students admitted into
first year from the academic year 2012-2013)

The M.Tech Degree of JNTU-KAKINADA shall be recommended to be conferred on candidates who are admitted to the program and fulfill all the requirements for the award of the Degree.

1.0 ELGIBILITY FOR ADMISSION:

Admission to the above program shall be made subject to the eligibility, qualifications and specialization as per the guidelines prescribed by the APSCHE and AICTE from time to time.

2.0 AWARD OF M.TECH. DEGREE:

a. A student shall be declared eligible for the award of the M.Tech. degree, if he pursues a course of study and completes it successfully for not less than two academic years and not more than four academic years.
b. A student, who fails to fulfill all the academic requirements for the award of the Degree within four academic years from the year of his admission, shall forfeit his seat in M.Tech. Course.
c. The duration of each semester will normally be 20 weeks with 5 days a week. A working day shall have 7 periods each of 50minutes.

3.0 COURSES OF STUDY:

M.TECH. COURSES	INTAKE
Chemical Engineering	18
Computer Science and Engineering	18
CAD/CAM	18
Infrastructural Engineering and Management	18
Structural Engineering	18
Power System Control and Automation	18
Embedded Systems & VLSI Design	18
Communications & Signal Processing	18
Software Engineering	18
Power Electronics & Drives	18
Computer Aided Analysis And Design (CAAD)	18

4.0 ATTENDANCE:

The attendance shall be considered subject wise.

a. A candidate shall be deemed to have eligibility to write end semester examinations in a subject if he has put in at least 75% of attendance in that subject.
b. Shortage of attendance up to 10% in any subject (i.e. 65% and above and below 75%) may be condoned by a Committee on genuine and valid reasons on representation by the candidate with supporting evidence.
c. Shortage of attendance below 65% shall in no case be condoned.
d. A student who gets less than 65% attendance in a maximum of two subjects in any semester shall not be permitted to takethe end- semester examination in which he/she falls short

His/her registration for those subjecWts will be treated as cancelled. The student should re-register and repeat those subjects as and when offered next.

e. If a student gets less than 65% attendance in more than two subjects in any semester he/she shall be detained and has to repeat the entire semester.

f. A stipulated fee shall be payable towards condonation of shortage of attendance.

5.0 EVALUATION:

The Performance of the candidate in each semester shall be evaluated subject-wise, with 100 marks for each theory subject and 100 marks for each practical, on the basis of Internal Evaluation and End Semester Examination.

a. A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

b. For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination, 40 marks shall be awarded based on the Internal Evaluation. One part of the internal evaluation shall be made based on the average of the marks secured in the two Mid–Term Examinations of 30 each conducted one in the middle of the Semester and the other immediately after the completion of instruction. Each mid-term examination shall be conducted for a duration of

120 minutes with 4 questions without any choice. The remaining 10 marks are awarded through an average of continuous evaluation of assignments / seminars / any other method, as notified by the teacher at the beginning of the semester.

c. For Practical subjects, 50 marks shall be awarded based on the performance in the End Semester Examinations, 50 marks shall be awarded based on the day-to-day performance as Internal marks**.** A candidate has to secure a minimum of 50% in

the external examination and has to secure a minimum of 50% on the aggregate to be declared successful.

d. There shall be a seminar presentation during III semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee. The Departmental Committee consists of the Head of the Department, supervisor and two other senior faculty members of the department. For Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful.

e. For Seminar in I, II Semesters in case of the course structure of having 5 Theory + 2 Labs. + 1 Seminar, a student has to deliver a seminar talk in each of the subjects in that semester which shall be evaluated for 10 marks each and average marks allotted shall be considered. A letter grade from A to C corresponding to the marks allotted may be awarded for the two credits so as to keep the existing structure and evaluation
undisturbed.

A – Excellent	(average marks > 8
B – Good	(6< average marks <8)
C – Satisfactory	(5< average marks <6)

If a satisfactory grade is not secured, one has to repeat in the following semester.

f. In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.0 a, c) he has to reappear for the End Examination in that subject.

A candidate shall be given one chance to re-register for each

subject provided the internal marks secured by a candidate are less than 50% and he has failed in the subject(s). In such a case the candidate must re-register for the subject (s) and secure required minimum attendance. Attendance in the re-registered subject (s) has to be calculated separately to become eligible to write the end- examination in the re-registered subject(s). In the event of re-registration, the internal marks and end examination marks obtained in the previous attempt are nullified.

g. In case the candidates secure less than the required attendance in any subject(s), he shall not be permitted to appear for the End Examination in that subject(s). He shall re-register for the subject(s) when next offered.

h. Laboratory examination for M.Tech subjects must be conducted with two Examiners, one of them being Laboratory Class Teacher and second examiner shall be other than Laboratory Teacher.

6.0 EVALUATION OF PROJECT / DISSERTATION WORK:

Every candidate shall be required to submit the thesis or dissertation after taking up a topic approved by the Departmental Research Committee (DRC).

a. A Departmental Research Committee (DRC) shall be constituted with the Head of the Department as the chairman and two senior faculty as members to oversee the proceedings of the project work from allotment to submission.

b. A Central Research Committee (CRC) shall be constituted with a Senior Professor as chair person, Heads of all the Departments which are offering the M.Tech. programmes and two other senior faculty members.

c. Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance

requirement of all the subjects (theory and practical subjects.)

d. After satisfying 6.0 c, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the DRC for its approval. Only after obtaining the approval of DRC the student can initiate the Project work

e. If a candidate wishes to change his supervisor or topic of the project he can do so with approval of DRC. However, the Departmental Project Review Committee shall examine whether the change of topic/supervisor leads to a major change in his initial plans of project proposal. If so, his date of registration for the Project work shall start from the date of change of Supervisor or topic as the case may be whichever is earlier.

f. A candidate shall submit and present the status report in two stages at least with a gap of 3 months between them after satisfying 6.0 d.

g. The work on the project shall be initiated in the beginning of the second year and the duration of the project is for two semesters. A candidate shall be permitted to submit his dissertation only after successful completion of all theory and practical subject with the approval of CRC but not earlier than 40 weeks from the date of registration of the project work. For the approval by CRC the candidate shall submit the draft copy of the thesis to the Principal through the concerned Head of the Department and shall make an oral presentation before the CRC.

h. Three copies of the dissertation certified by the supervisor shall be submitted to the College after approval by the CRC.

i. The dissertation shall be adjudicated by one examiner selected by the Principal. For this HOD shall submit in consultation with the supervisor a panel of 5 examiners, who are experienced in that field.

i. If the report of the examiner is not favorable, the candidate shall revise and resubmit the dissertation, in a time frame as prescribed by the CRC. If the report of the examiner is unfavorable again, the dissertation shall be summarily rejected then the candidate shall change the topic of the Project and option shall be given to change the supervisor also.

j. If the report of the examiner is favorable, viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the Department and the examiner who adjudicated the dissertation. The Board shall jointly report candidate's work as:

A. Excellent
B. Good
C. Satisfactory

7.0 AWARD OF DEGREE AND CLASS :

A candidate shall be eligible for the respective degree if he satisfies the minimum academic requirements in every subject and secures satisfactory or higher grade report on his dissertation and viva-voce. After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M.Tech. Degree he shall be placed in one of the following three classes.

% of Marks secured	Class Awarded
70% and above	First Class with Distinction
60% and above but less than 70%	First Class
50% and above but less than 60%	Second Class

The marks in internal evaluation and end examination shall be shown separately in the marks memorandum.

The grade of the dissertation shall also be mentioned in the marks memorandum.

8.0 WITHHOLDING OF RESULTS:

If the candidate has not paid any dues to the college or if any case of indiscipline is pending against him, the result of the candidate will be withheld and he will not be allowed into the next higher semester. The recommendation for the issue of the degree shall be liable to be withheld in such cases.

9.0 TRANSITORY REGULATIONS:

A candidate who has discontinued or has been detained for want of attendance or who has failed after having studied the subject is eligible for admission to the same or equivalent subject(s) as and when subject(s) is/are offered, subject to 6.0 e and 2.0

10.0 GENERAL

1. The academic regulations should be read as a whole for purpose of any interpretation.

2. In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman Academic Council is final

3. The College may change or amend the academic regulations and syllabus at any time and the changes amendments made shall be applicable to all the students with effect from the date notified by the College.

4. Wherever the word he, him or his occur, it will also include she, hers.

COURSE STRUCTURE

I SEMESTER

COURSE CODE	THEORY/LAB	L	P	C
10EC2201	Communication Theory	4	-	4
10EC2202	Digital Data Communications	4	-	4
10EC2203	Coding Theory and Practice	4	-	4
10EC2204	Transform Techniques	4	-	4
10EC2205	Digital Signal Processing	4	-	4
	Elective I	4	-	4
10EC2206	VLSI Technology & Design			
10EC2207	Microcontroller Applications			
10EC2208	Digital Signal Processing Lab		3	2
	Total	**24**	**3**	**26**

II SEMESTER

COURSE CODE	THEORY/LAB	L	P	C
10EC2209	Wireless Communications & Networks	4	-	4
10EC2210	Fiber Optical Communication System	4	-	4
10EC2211	Computer Networks	4	-	4
10EC2212	Advanced Digital Signal Processing	4	-	4
10EC2213	DSP Processors and Architecture	4	-	4
	Elective-II	4	-	4
10EC2214	Image Processing			4
10EC2215	Embedded System Concepts			
10EC2216	Advanced Communication Lab		3	2
	Total	**24**	**3**	**26**

III SEMESTER

COURSE CODE	THEORY/LAB	L	P	C
	Commencement of Project Work			
10EC22S1	SEMINAR	**-**	**-**	**2**

IV SEMESTER

COURSE CODE	THEORY/LAB	L	P	C
10EC2217	PROJECT WORK DISSERTATION / THESIS EXCELLENT/GOOD/SATISFACTORY/ NON-SATISFACTORY	**-**	**-**	**56**

COMMUNICATION THEORY

Course Code: 10EC2201

L	P	C
4	0	4

UNIT – I

Review of Fourier Techniques in Communication (Including Hilbert transforms and representation of band pass signals). **Probability and Random processes:** Random variables, pdf and c.d.f, expected values: transformation of variables in one and two dimensions. Characterization of a random process: Stationary; ensemble averages; systems with random signal excitation; Gaussian processes; electrical noise.

UNIT – II

Analog Communications

Mathematical treatment of Linear (AM, DSB-SC, SSB and VSB) and exponential (PM and FM) modulation; spectra of angle modulated signals; Noise performance of linear and exponential modulated signals; PE and DE in FM.

UNIT-III

Introduction to Digital Communication

Sampling of low-pass and band-pass signals; quantization ; PAM, Bennet's formula; Log-PCM; base band digital communication; Nyquist pulse shaping, spectra analysis of some important line codes.

UNIT-IV

Digital Modulation Schemes

Representation of digital signal waveforms, Introduction to digital modulation schemes- ASK, PSK and FSK; Digital demodulation and the optimal receiver, performance of digital communication systems in the presence of noise, coherent quadrature modulation techniques.

UNIT-V

Detection and Estimation Theory

Binary hypothesis testing, Bayes, Minimax and Neyman-Pearson tests; Bayesian parameter estimation, MMSE, MMAE and MAP estimation procedures.

UNIT-VI

Spread Spectrum Modulation

Spread spectrum modulation: Introduction, DS Spread spectrum, use of Spread spectrum with CDMA, Ranging using DS Spread spectrum, FH Spread spectrum, PN sequences, Acquisition and tracking of FH & DS signals.

UNIT-VII

Introduction to OFDM

The principles of OFDM, FDM modulation system, orthogonality and OFDM, Transmitter and Receiver sections, multi path channels and the use of cyclic prefix, ISI, coded OFDM, Non ideal effects in an OFDM, benefits and applications.

UNIT-VIII

Information Theory

Concept of amount of information, average information, Entropy, information rate Shannon's theorem, channel capacity: BSC and Gaussian channel, Tradeoff between bandwidth and SNR, optimal coding techniques; Shannon Fanon coding, Huffman coding.

Text Books:

1. John G. Proakis and Masoud Salehi, "Communication Systems Engineering," Prentice-Hall, 2nd Edition, 2002.
2. Proakis and Salehi, "Fundamentals of Communication Systems", Prentice Hall.,1st edition,2005
3. Stern & Mahmoud, "Communication Systems", Prentice Hall.
4. M. Simon, S. Hinedi, and W. Lindsey, "Digital Communication Techniques," Prentice-Hall, 1995.

References:

1. B.P.Lathi , "Modern Analog and Digital Communication", Oxford reprint, 3rd Edition, 2004.

2. H.Tanb and D.Schiling, "Principles of Communication systems", TMH 2003

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DIGITAL DATA COMMUNICATIONS

Course Code: 10EC2202

L	P	C
4	0	4

UNIT- I
Digital Modulation Techniques
FSK, MSK, BinaryPSK, M-aryPSK, M-aryQAM, DPSK Methods, Bandwidth efficiency, Carrier recovery, Clock recovery.

UNIT- II
Data Communication Methods
Data Communication Circuits, point-to-point, Multi-point configurations and Topologies, Broadcasting, multicasting configuration, transmission modes, 2-wire and 4-wire operations, Codes, Error detection methods, Error correction methods, Character synchronization.

UNIT- III
Data Communication Protocols
Asynchronous protocols, Synchronous protocols, Bisync Protocol, SDLC, HDLC-Frame format, ATM Frame format, Flow control and error control.

UNIT- IV
Switching Techniques
Circuit Switching, Message Switching and Packet Switching principles, Virtual circuit and datagram techniques, X.25 and frame relay.

UNIT- V
Line Protocals and Congestion Control
Line protocols: Basic mode, Half-duplex point-to-point protocol, Half-Duplex Multi-Point Protocol, Full-Duplex Protocols, Polling, Roll Call and Hub Polling, Traffic management, Congestion control in packet switching networks and Frame relay.

UNIT- VI

Digital Multiplexing-I

TDM, T1, E1 carrier systems, CCITT-TDM carrier system, CODEC chips, Digital hierarchy, Line Encoding, Frame Synchronization.

UNIT- VII

Digital Multiplexing-II

Multiplexers, Statistical multiplexer, Concentrator, front-end communication processor, Digital PBX, long haul communication with FDM, Hybrid data.

UNIT- VIII

Optical Networks

Basic Optical Network Topologies and their performances, SONET/SDH – Transmission formats and Speeds, Optical interfaces, SONET/SDH rings and networks.

Text Books

1. W. TOMASI: Advanced Electronic Communications Systems, PHI.,4th edition.
2. William Stallings "Data and Computer Communications", PEI, 7/e.
3. B.Gerd Keiser, "Optical Communications", PHI,4th edition.

References

1. T. HOUSELY: Data Communications and Teleprocessing Systems, PHI.,2nd edition.
2. B.A.Forouzon, " Data and Computer Networking Communications", 3rd TMH.

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CODING THEORY & PRACTICE

Course Code: 10EC2203

L	P	C
4	0	4

UNIT- I

Information Theory

Entropy, Information rate, source coding : Shannon-Fano and Huffman coding techniques, Mutual Information, Channel capacity of Discrete Channel, Shannon- Hartly law, Trade-off between bandwidth and SNR.

UNIT- II

Introduction and Overview Error Control Codes

Examples of the use of error control codes, basic notations, coding gain, Characterization of Error control codes, performance of error control codes, comparison of uncoded and coded systems.

UNIT- III

Convolution Codes

Convolution encoders, structural properties of convolution codes, Trellis Diagrams, Viterbi Algorithm, Performance Analysis.

UNIT- IV

Linear Block Codes

Linear block Codes and their properties, standard arrays, Syndromes, Weight Distribution. Error Detection/Correction Properties, Modified Linear block codes.

UNIT- V

Finite Fields

Groups, Rings, Fields Properties of finite Fields, Extension Fields, Polynomials over Finite Fields, Minimal Polynomials, Conjugates.

UNIT- VI

Cyclic Codes

General theory, Shift Register Implementations, Shortened Cyclic codes, CRCs for Error Detection.

UNIT- VII

Bch And Rs Codes

Algebraic Description, Frequency Domain Description, Decoding Algorithms for BCH and RS Codes.

UNIT- VIII

Applications

Concatenated Codes, Interleaves, The Compact Disc, Codes for Magnetic recording.

Text Books

1. Stephen B.Wicker Error Control Systems for Digital Communication and storage, Prentice Hall. 1995ISBN 0-13-200809-2
2. Kennedy, Electronic Communication systems, Mc Graw Hill.,4th Edition.

Reference Books

1. John Proakis, Digital Communications, TMH.
2. Simon Haykin, Communication System,5th edition, Jhon willey, 2011

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TRANSFORM TECHNIQUES

Course Code: 10EC2204

L	P	C
4	0	4

UNIT- I

Introduction

Orthogonal signal spaces, approximations of functions by a set of mutually orthogonal functions, Orthogonality in complex functions, trigonometric & exponential Fourier series, Hilbert Transforms, Properties and applications.

UNIT- II

Two Dimensional Fourier Transforms and Its Applications

Concept of Two Dimensional Fourier transforms- properties & their significance, energy & power spectral density functions.

UNIT- III

Two Dimentional Transforms and Its Applications-I

Walsh transforms, Hadamard transform, Discrete Cosine Transforms, Haar Transforms.

UNIT- IV

Two Dimentional Transforms and Its Applications-II

Slant, KL transforms, Hough Transforms, Radon Transforms.

UNIT- V

Other Transforms

Short time Fourier transforms & properties of STFT, continuous wavelet transforms, Inverse CWT.

UNIT- VI

Discrete Wavelet Transforms

Introduction to discrete wavelet transforms & orthogonal wavelet decomposition.

UNIT- VII

Multi-Resolution Analysis

Multi-Resolution Analysis (MRA), Two scale relations, Orthogonal wavelets, their relationship to filter banks, PR QMF filter banks.

UNIT- VIII

Introduction to Various Wavelets

Alternate wavelet representations.

Text Books:

1. B.P.lathi, "Signals & systems", BS Publishers 1/e, 2004.
2. Raghuveer. M.rao, ajit S, "Wavelet transforms – Introduction to theory & applications", pearson publications, 1st edition, 2006.
3. A.K.Jain, "Fundamentals of Digital image processing", 2/e Pearson.

Reference Books:

1. C. Gonzalez & Redwoods "Digital Image Processing" 1/e, 2001.
2. Jaideva C.Goswami, Andrew K.Chan, John Willey & Sons. "Fundamentals of wavelets -Theory, Algorithms & applications".

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DIGITAL SIGNAL PROCESSING

Course Code: 10EC2205

L	P	C
4	0	4

UNIT- I

Introduction

Introduction to Digital Signal Processing: Discrete time signals & sequences, linear shift invariant systems, stability, and causality. Linear constant coefficient difference equations, Frequency domain representation of discrete time signals and systems.

UNIT- II

Discrete Fourier Series

Properties of discrete Fourier series, DFS representation of periodic sequences, Discrete Fourier transforms: Properties of DFT, linear convolution of sequences using DFT, Computation of DFT. Relation between Z-transform and DFS.

UNIT- III

Fast Fourier Transforms

Fast Fourier transforms (FFT) - Radix-2 decimation in time and decimation in frequency FFT Algorithms, Inverse FFT, and FFT for composite N.

UNIT- IV

Realization of Digital Filters

Review of Z-transforms, Applications of Z – transforms, solution of difference equations of digital filters, Block diagram representation of linear constant-coefficient difference equations, Basic structures of IIR systems, Transposed forms, Basic structures of FIR systems, System function.

UNIT- V

IIR Digital Filters

Analog filter approximations – Butter worth and Chebyshev, Design of IIR Digital filters from analog filters, Design Examples: Analog-Digital transformations.

UNIT- VI

FIR Digital Filters

Characteristics of FIR Digital Filters, frequency response, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR & FIR filters.

UNIT- VII

Multirate Digital Signal Processing

Decimation, interpolation, sampling rate conversion, Implementation of sampling rate conversion.

UNIT- VIII

Introduction To Dsp Processors

Introduction to programmable DSPs: Multiplier and Multiplier Accumulator (MAC), Modified Bus Structures and Memory Access schemes in DSPs Multiple access memory, multiport memory, VLSI Architecture, Pipelining, Special addressing modes, On-Chip Peripherals. Architecture of TMS 320C5X- Introduction, Bus Structure, Central Arithmetic Logic Unit, Auxiliary Registrar, Index Registrar, Auxiliary Register Compare Register, Block Move Address Register, Parallel Logic Unit, Memory mapped registers, program controller, Some flags in the status registers, On- chip registers, On-chip peripherals.

Text Books

1. John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing, Principles, Algorithms, and Applications", Pearson Education / PHI, 2007.
2. A.V.Oppenheim and R.W. Schaffer, "Discrete Time Signal Processing" PHI.

3.B.Venkataramani,M.Bhaskar,Digital,"Signal Processors- Architecture, Programming and Applications", TATA McGraw Hill, 2002.

Reference Books:

1. Andreas Antoniou, "Digital Signal Processing:", TATA McGraw Hill, 2006.
2. MH Hayes, "Digital Signal Processing: Schaum's Outlines, TATA Mc-Graw Hill, 2007.
3. C. Britton Rorabaugh, "DSP Primer", Tata McGraw Hill, 2005.
4. Robert J. Schilling, Sandra L. Harris & Thomson, "Fundamentals of Digital Signal Processing using Matlab" 2007.
5. Digital Signal Processing Alan V. Oppenheim, Ronald W. Schafer, PHI Ed, 2006.
6. S.K.Mithra, "Digital Signal Processing", TMH, 3rd edition, 2009.

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VLSI TECHNOLOGY & DESIGN

Course Code: 10EC2206

L	P	C
4	0	4

UNIT- I

Review of Microelectronics and Introduction to MOS Technologies

(MOS, CMOS, Bi CMOS) Technology trends and projections.

UNIT- II

Basic Electrical Properties of MOS, CMOS & Bi-COMS Circuits

Ids-Vds relationships, Threshold voltage V_t, G_m, G_{ds} and W_o, Pass Transistor, MOS, CMOS &

Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT- III

Layout Design and Tools

Transistor structures, Wires and Vias , Scalable Design rules ,Layout Design tools.

UNIT- IV

Logic Gates & Layouts

Static complementary gates, switch logic, Alternative gate circuits , low power gates, Resistive and Inductive interconnect delays.

UNIT- V

Combinational Logic Networks

Layouts, Simulation, Network delay, interconnect design, power optimization, Switch logic networks, Gate and Network testing.

UNIT- VI

Sequential Systems

Memory cells and Arrays, clocking disciplines, Design, power optimization, Design validation and testing.

UNIT- VII

Floor Planning & Architecture Design

Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

UNIT- VIII

Introduction to CAD Systems (Algorithms) and Chip Design

Layout Synthesis and Analysis, Scheduling and printing; Hardware/Software Co-design, chip design methodologies- A simple Design example.

Text Books:

1. K.Eshraghian et. al(3 authors) "Essentials of VLSI Circuits and Systems", PHI of India Ltd, 2005.
2. Wayne Wolf, "Modern VLSI Design", Pearson Education, 3rd Edition, fifth Indian Reprint,2005.

References:

1. N.H.E Weste, K.Eshraghian, Adison Wesley, "Principals of CMOS Design", 2nd Edition.
2. Fabricius, "Introduction to VLSI Design", MGH International Edition, 1990.
3. Baker & Li Boyce, "CMOS Circuit Design, Layout and Simulation", PHI, 2004.

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MICROCONTROLLER AND APPLICATIONS

Course Code : 10EC2207

L	P	C
4	0	4

UNIT- I

Overview Of Architecture and Microcontroller Resources

Architecture of a microcontroller – Microcontroller resources – Resources in advanced and next generation microcontrollers – 8051 microcontroller – Internal and External memories – Counters and Timers – Synchronous serial-cum-asynchronous serial communication - Interrupts.

UNIT- II

8051 Family Microcontrollers Instruction Set

Basic assembly language programming – Data transfer instructions – Data and Bit manipulation instructions – Arithmetic instructions – Instructions for Logical operations on the tes among the Registers, Internal RAM, and SFRs – Program flow control instructions – Interrupt control flow.

UNIT- III

Real Time Control

Interrupts, Interrupt handling structure of an MCU – Interrupt Latency and Interrupt deadline – Multiple sources of the interrupts – Non-maskable interrupt sources – Enabling or disabling of the sources – Polling to determine the interrupt source and assignment of the priorities among them – Interrupt structure in Intel 8051.

UNIT- IV

Real Time Control Timers

Programmable Timers in the MCU's – Free running counter and real time control – Interrupt interval and density constraints.

UNIT- V

Systems Design

Digital and Analog Interfacing Methods, Switch, Keypad and Keyboard interfacings – LED and Array of LEDs – Keyboard-cum-Display controller (8279) – Alphanumeric Devices – Display Systems and its interfaces – Printer interfaces – Programmable instruments interface using IEEE 488 Bus – Interfacing with the Flash Memory – Interfaces – Interfacing to High Power Devices – Analog input interfacing – Analog output interfacing – Optical motor shaft encoders – Industrial control – Industrial process control system – Prototype MCU based Measuring instruments – Robotics and Embedded control – Digital Signal Processing and Digital Filters.

UNIT- VI

Real Time Operating System for Micro Controllers

Real Time operating system – RTOS of Keil (RTX51) – Use of RTOS in Design – Software development tools for Microcontrollers.

UNIT- VII

16-Bit Microcontrollers

Hardware – Memory map in Intel 80196 family MCU system – IO ports – Programmable Timers and High-speed outputs and input captures – Interrupts – instructions.

UNIT- VIII

ARM 32 Bit MCUs

Introduction to 16/32 Bit processors – ARM architecture and organization – ARM / Thumb programming model – ARM / Thumb instruction set – Development tools.

Text Books:

1. Raj Kamal, "Microcontrollers Architecture, Programming, Interfacing and System Design", Pearson Education, 2005.
2. Mazidi and Mazidi, "The 8051 Microcontroller and Embedded Systems", PHI, 2000.

Reference Books:

1. A.V. Deshmuk, “Microcontrollers (Theory & Applications)”, WTMH 2005.
2. John B. Peatman, “Design with PIC Microcontrollers”, Pearson Education, 2005.

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DIGITAL SIGNAL PROCESSING LAB

Course Code: 10EC2208

L	P	C
0	3	2

1. Write a program for linear convolution of two sequences.

2. Write a program for circular convolution.

3. Write a program to perform linear convolution using circular convolution.

4. Write a program to perform N-point DFT. Also perform the IDFT on the result obtained to verify the result.

5. Write a program to perform circular correlation using
a) Direct method b) circular convolution using rotation method.

6. Write a program to perform circular convolution and correlation using DFT.
7. Write a program to perform linear convolution using (a) overlap save method (b) overlap add method.

8. Write a program to perform FFT on a sequence using the following methods. (a) Decimation in time (b) Decimation in frequency

9. Write a program to perform IDFT on a transformed sequence using DFT.
10. Write a program to design an FIR filter using windowing technique.

11. Write a program to design an IIR filter using (a) impulse invariant method (b) bilinear transformation method.

WIRELESS COMMUNICATIONS AND NETWORKS

Course Code: 10EC2209

L	P	C
4	0	4

UNIT- I

Multiple Access Techniques for Wireless Communication:

Introduction, FDMA, TDMA, Spread Spectrum, Multiple access, SDMA, Packet radio, Packet radio protocols, CSMA protocols, Reservation protocols.

UNIT- II

Introduction to Wireless Networking:

Introduction, Difference between wireless and fixed telephone networks, Development of wireless networks, Traffic routing in wireless networks.

UNIT- III

Wireless Data Services:

CDPD, ARDIS, RMD, Common channel signaling, ISDN, BISDN and ATM,SS7, SS7 user part, signaling traffic in SS7.

UNIT- IV

Mobile IP and Wireless Access Protocol:

Mobile IP Operation of mobile IP, Co-located address, Registration, Tunneling, WAP Architecture, overview, WML scripts, WAP service, WAP session protocol, wireless transaction, Wireless datagram protocol.

UNIT- V

Wireless LAN Technology:

Infrared LANs, Spread spectrum LANs, Narrow bank microwave LANs, IEEE 802 protocol Architecture, IEEE802 architecture and services, 802.11 medium access control, 802.11
physical layer.

UNIT- VI

Blue Tooth:

Overview, Radio specification, Base band specification, Links manager specification, Logical link control and adaptation protocol. Introduction to WLL Technology.

UNIT- VII

Mobile Data Networks:

Introduction, Data oriented CDPD Network, GPRS and higher data rates, Short messaging service in GSM, Mobile application protocol.

UNIT- VIII

Wireless ATM & Hiper LAN:

Introduction, Wireless ATM, HIPERLAN, Adhoc Networking and WPAN.

Text Books:

1. Theodore, S.Rappaport, "Wireless Communications, Principles, Practice", PHI, 2nd Edn., 2002.
2. William Stallings, "Wireless Communication and Networking", PHI, 2nd edition, 2003.

References:

1. Kamilo Feher, "Wireless Digital Communications", PHI, 2002.
2. Kaveh Pah Laven and P. Krishna Murthy, "Principles of Wireless Networks" Pearson Education, 2002.
3. Andreaws F. Molisch, "Wireless Communications",Wiley India, 2006.
4. Dharma Prakash Agarwal, Qing-An Zeng, "Introduction to Wireless and Mobile Systems", Thomson 2nd Edition, 2006.

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FIBER OPTICAL COMMUNICATION SYSTEMS

Course Code: 10EC2210

L	P	C
4	0	4

UNIT-I

Introduction

Historical development, the general system, advantages of OFC, Ray theory transmission-total internal reflection, acceptance angle, numerical aperture, skew rays, fiber materials-glass fibers, halide glass fibers, active glass fibers, plastic clad glass fibers, plastic fibers.

UNIT-II

Optic Fiber Waveguides

Step – Index Fiber, Graded – Index Fiber, Modes in Step-Index Fibers, Modes in Graded – Index Fibers, Pulse Distortion and Information Rate in Optic Fibers, Construction of Optic Fibers, Optic Fiber Cables.

UNIT-III

Signal degradation in optical fibers

Attenuation-absorption, scattering, radiation losses, intramodal and intermodal dispersion, polarization mode dispersion.

UNIT-IV

Light Sources and Detectors

Light-Emitting Diodes, Light-Emitting – Diodes Operating Characteristics, Laser Principles, Laser Diodes, Laser-Diode Operating Characteristics, Distributed – Feedback Laser Diode, Optical Amplifiers, Fiber Laser, Vertical-Cavity Surface-Emitting Laser Diodes, Principles of Photodetection, Photomultiplier, Semiconductor Photodiode, PIN Photodiode, Avalanche Photodiode.

UNIT-V

Couplers and Connectors

Connector Principles, Fiber end Preparation, Splices, Connectors, Source Coupling, Distribution Networks and Fiber Components, Distribution Networks, Directional Couplers, Star Couplers, Switches, Fiber Optical Isolator, Wavelength-Division Multiplexing, Fiber Bragg Gratings, Other Components : Attenuator, Circulator and Polarization Controller.

UNIT-VI

Modulation, Noise and Detection

Light-Emitting-Diode Modulation and Circuits, Laser-Diode Modulation and Circuits, Analog-Modulation Formats, Digital-Modulation Formats, Optic Heterodyne Receivers, Thermal and Shot Noise, Signal-to-Noise Ratio, Error Rates, Modal Noise, Amplifier Noise, Laser Noise, and Jitter, Additional Noise Contributors, receiver Circuit Design.

UNIT-VII

System Design and Fiber Optical Applications

Analog System Design, Digital System Design, Applications of Fiber Optics-public network applications, military applications, civil, consumer and industrial applications.

UNIT-VIII

Optical fiber measurements

Introduction, measurement of attenuation, dispersion, refractive index profile, numerical aperture, diameter and field.

Text Books:

1. Joseph. C. Palais, “Fiber Optic Communications”, Pearson Education, Asia, 2002.
2. John M Senior, “Optical Fiber Communications, principles and practice”, II edition.

Reference Books:

1. John Powers, “Fiber Optic Systems”, Irwin Publications, 1997.
2. Howes M.J., Morgen & D.V John Wiely, “Optical Fiber Communication”.
3. Gerd Keiser, “Optical fiber Communications”, TMH.,2nd edition, 199.

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COMPUTER NETWORKS

Course Code: 10EC2211

L	P	C
4	0	4

UNIT- I
Introduction
OSI, TCP/IP and other networks models, Examples of Networks: Novell Networks, Arpanet, Internet, Network Topologies WAN, LAN, MAN.

UNIT- II
Physical Layer
Transmission media copper, twisted pair wireless, switching and encoding asynchronous communications; Narrow band, broad band ISDN and ATM.

UNIT- III
Data Link Layer
Design issues, framing, error detection and correction, CRC, Elementary Protocol-stop and wait, Sliding Window, Slip, Data link layer in HDLC, Internet, ATM.

UNIT-
Medium Access Sub Layer
ALOHA, MAC addresses, Carrier sense multiple access, IEEE 802.X Standard Ethernet, wireless LANS, Bridges.

UNIT- V
Network Layer
Virtual circuit and Datagram subnets-Routing algorithm shortest path routing, Flooding, Hierarchical routing, Broad cast, Multi cast, distance vector routing.

UNIT- VI

Dynamic Routing

Broadcast routing. Rotary for mobility, Congestion, Control Algorithms – General Principles of Congestion prevention policies. Internetworking: The Network layer in the internet and in the ATM Networks.

UNIT- VII

Transport Layer

Transport Services, Connection management, TCP and UDP protocols; ATM AAL Layer Protocol.

UNIT- VIII

Application Layer

Network Security, Domain name system, SNMP, Electronic Mail; the World WEB, Multi Media.

Text Books :

1. Andrew S Tanenbaum, "Computer Networks", Pearson Education/PHI 4th Edition.
2. Behrouz A. Forouzan, "Data Communications and Networking", Third Edition TMH.,4th edition-2006.

References

1. S.Keshav, "An Engineering Approach to Computer Networks", 2nd Edition, Pearson Education.
2. W.A.Shay, Thomson**, "**Understanding communications and Networks, 3rd Edition.

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ADVANCED DIGITAL SIGNAL PROCESSING

Course Code: 10EC2212

L	P	C
4	0	4

UNIT- I

Discrete Fourier Transforms

Properties of DFT, Linear Filtering methods based on the DFT, Overlap-save, Overlap -Add methods, frequency analysis of signals.

UNIT- II

Fast Fourier Transforms

Radix-2 FFT and Split- Radix FFT algorithms The Goertzel and Chirp Z transform algorithms.

UNIT- III

Design Of Iir Filters

Design of IIR filters using Butterworth & Chebyshev approximations, frequency transformation techniques, structures for IIR systems – cascade, parallel, lattice & lattice-ladder structures.

UNIT- IV

Design of Fir Filters

Fourier series method, Windowing techniques, design of digital filters based on least – squares method, pade approximations, least squares design, wiener filter methods, structures for FIR systems –cascade, parallel, lattice & lattice-ladder structures.

UNIT- V

Multi Rate Signal Processing

Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

UNIT- VI

Power Spectral Estimation

Estimation of spectra from finite duration observation of signals, Non-parametric methods: Bartlett, Welch & Blackmann & Tukey methods.

UNIT- VII

Parametric Methods for Power Spectrum Estimation

Relation between auto correlation & model parameters, Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT- VIII

Analysis of Finite Wordlength Effects in Fixed-Point DSP Systems

Fixed, Floating Point Arhimetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

Text Books:

1. J.G.Proakis & D.G.Manolokis, "Digital Signal Processing –Principles, Algorithms Applications" PHI.,2nd edition-2009
2. Alan V Oppenheim & Ronald W Schaffer, "Discrete Time signal processing", PHI.,Second Impression - 2007
3. Emmanuel C.Ifeacher Barrie. W. Jervis, "DSP -A Pratical Approach", Pearson Education

References

1. S. M .Kay, "Modern spectral Estimation Techniques", PHI, 1997.

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DSP PROCESSORS AND ARCHITECTURES

Course Code: 10EC2213

L	P	C
4	0	4

UNIT- I

Introduction to Digital Signal Processing

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT- II

Computational Accuracy in DSP Implementations

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT- III

Architectures for Programmable DSP Devices

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT- IV

Execution Control and Pipelining

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT- V

Programmable Digital Signal Processors

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT- VI

Implementations of Basic DSP Algorithms

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT- VII

Implementation of FFT Algorithms

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT- VIII

Interfacing Memory and I/O Peripherals to Programmable DSP Devices

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O,

Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

Text Books:

1. Avtar Singh and S. Srinivasan, "Digital Signal Processing", Thomson Publications, 2004.
2. Lapsley et al. S. Chand & Co, "DSP Processor Fundamentals, Architectures & Features", 2000.

References :

1. B. Venkata Ramani and M. Bhaskar, "Digital Signal Processors, Architecture, Programming and Applications", TMH, 2004. (10^{th} Print, 2007)
2. Jonatham Stein, John Wiley "Digital Signal Processing". (reprint – 2009)

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IMAGE PROCESSING

Course Code: 10EC2214

L	P	C
4	0	4

UNIT- I

Image Processing Fundamentals

Image Transforms – Fourier Transform, Walsh, Handamard, DCT, Haar, Slant, KL transforms and their properties.

UNIT- II

Image Enhancement

Enhancement by point processing, Histogram Processing, Enhancement in Spatial domain and in Frequency domain.

UNIT- III

Color Image Processing

Fundamentals – Models – Pseudo Color image processing – Basics – Converting to other color spaces – Transformations - Color Smoothing and Sharpening – Color Segmentation – Noise – Color Noise Compression.

UNIT- IV

Image Filtering and Restoration

Degradation Model – Diagnolisation of Circulant and Block Circulant Matrices – Algebraic approach to restoration- Inverse filtering – LMS Restoration – Constrained least Squares and iterative restoration, Geometric Transformations.

UNIT- V

Image Compression

Fundamentals – Compression Models – Lossless and Lossy compressions – Compression Standards.

UNIT- VI

Image Segmentation and Edge Detection

Detection of discontinuities – Edge linking and boundary detection – Region oriented segmentation – use of motion in segmentation – Marr-Hildreth Edge Detection – Canny Detectors.

UNIT- VII

Representation and Description

Various schemes – Boundary Descriptors – Regional Descriptors.

UNIT -VIII

Morphological Image Processing

Preliminaries – Dilation & Erosion – Opening & Closing – Hit-Miss Transformation – Morphological algorithms – Extension to Grey Scale Images

Text Books:

1. Rafael C.Gonzalez, Richard E. Woods, "Digital Image Processing", Pearson education, 2nd Edition, 3rd Edition, 2008.
2. Rafael C.Gonzalez, Richard E.Woods, Steven L.Edding, "Digital Image Processing Using MATLAB", Pearson Education, 2nd Edition. (5th impression – 2009)

References:

1. A.K.Jain, "Fundamentals of Digital Image Processing", PHI.
2. William K.Prah, John wilely, "Digital Image Processing", 3rd Edition,2004.
3. Weeks Jr, SPIC/IEEE series, "Fundamentals of Electronic Image Processing" PHI.

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EMBEDDED SYSTEMS CONCEPTS

Course Code : 10EC2215

L	P	C
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UNIT- I

Introduction to Embedded Systems

Embedded system, processor in the system, other hardware units, software embedded into a system, exemplary embedded systems, embedded system – on – chip (SOC) and in VLSI circuit.

UNIT- II

Processor and Memory Organization

Structural units in a Processor, Processor selection for an embedded system, memory devices, memory selection for an embedded systems, allocation of memory to program cache and memory management links, segments and blocks and memory map of a system, DMA, interfacing processors, memories and Input Output Devices.

UNIT- III

Devices and Buses for Device Networks

I/O devices, timer and counting devices, serial communication using the 'I2 C',' CAN and advanced I/O buses between the networked multiple devices, host systems or computer parallel communication between the networked I/O multiple devices using the ISA, PCI, PCI-X and advanced buses.

UNIT- IV

Device Drivers and Interrupts Servicing Mechanism

Device drivers, parallel port and serial port device drivers in a system, device drivers for internal programmable timing devices, interrupt servicing mechanism.

UNIT- V

Programming Concepts and Embedded Programming in C and C++

Software programming in assembly language(ALP) and in high level language 'C','C' program elements: header and source files and preprocessor directives, program elements: macros and functions, data types ,data structures, modifiers , statements , loop and pointers, queues ,stacks , lists and ordered lists, embedded programming in C++, embedded programming in java,'C' program compiler and cross-compiler , source code engineering tools for embedded C/C++,optimization of memory needs.

UNIT- VI

Program Modelling Concepts in Single and Multi Processor Systems Software - Development Process

Modeling processes for software analysis before software implementation, programming models for event control or response time constrained real time programs, modeling of multi processor systems.

UNIT- VII

Hardware and Software Co Design - I

Embedded System project development, embedded System design and co-design issues in system development process, design cycle in the development phase for an Embedded System.

UNIT- VIII

Hardware and Software Co Design – II

Use of target system or its Emulator and In-Circuit Emulator (ICE), use of Software tools for Development of an Embedded System, use of scopes and logic analyzers for System Hardware Tests

Text Book:

1. Rajkamal, "Embedded systems: Architecture, programming and Design" by TMH., 2nd Edition, (5th reprint – 2010)

References:

1. Arnold S Burger, “Embedded system Design” CMP, 2009
2. David Simon, “An embedded Software Primer”, PEA, (6th Impression - 2008).
3. Steve Heath; Butterworth Heinenann, Newton mass, “Embedded Systems Design: Real world design”, USA 2002, 2nd Edition 2003.
4. Hayt “Data communication”.

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ADVANCED COMMUNICATION LAB

Course Code: 10EC2216

L	P	C
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1. To study Time division multiplexing.

2. To study PCM.

3. To study the different channel coding and decoding technique.

4. Generation and reception of different types of signals like ASK, PSK, FSK.

5. To transmit and receive three separate signal audio, video, tone simultaneously through satellite link.

6. To transmit PC data through satellite link using a satellite communication demonstration unit.

7. Experimentally compare different forms of BPSK, QPSK, OQPSK and analyze their spectrum with spectrum analyzer.

8. Spreading and dispreading using additive white Gaussian noise generation/ Gold code and other forms of spreading techniques.

9. Transmit different types of signals suing a ISDN system.

10. Analyze the process of data communication in LAN using LAN trainer and compare the performance different media access techniques.

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