

**ACADEMIC REGULATIONS**  
**COURSE STRUCTURE AND SYLLABI**  
**FOR**  
**M.TECH.**  
**EMBEDDED SYSTEMS & VLSI DESIGN**  
**(Electronics and Communication Engineering)**  
**2012-2013**



**COLLEGE OF ENGINEERING**  
**(AUTONOMOUS)**

**GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING**  
**(AUTONOMOUS)**  
**ACCREDITED BY NAAC WITH A GRADE WITH A CGPA OF 3.47/4.00**  
**AFFILIATED TO JNTU KAKINADA**  
**MADHURAWADA, VISAKHAPATNAM 530048**



## *Vision*

*To evolve into and sustain as a Centre of  
Excellence in Technological Education  
and Research with a holistic approach.*

## *Mission*

*To produce high quality engineering graduates with the requisite theoretical and practical knowledge and social awareness to be able to contribute effectively to the progress of the society through their chosen field of endeavor.*

*To undertake Research & Development, and extension activities in the fields of Science and Engineering in areas of relevance for immediate application as well as for strengthening or establishing fundamental knowledge.*

## FOREWORD

*It is three years since the G.V.P College of Engineering has become Autonomous with the appreciation and support of erstwhile JNTU and the fast growing new JNTU-K. The college is progressing well with its programmes and procedures drawing more and more accolades from its sister autonomous colleges and higher authorities. The student community, also could adjust well to the new system without any acrimony.*

*The College is enriched with the experience of running the Post-graduate programmes under Autonomous stream. It is a moment of pride and achievement that the first Autonomous batch of M.Tech in some branches left the college to the satisfaction of all concerned including firms visited the campus for placements.*

*Another larger than canvas picture is foreseen for the programmes wherein the college is getting the funds through TEQIP - II for up-scaling the PG education and research under sub- component 1.2. In this connection two new PG Programmes have been introduced in Mechanical, Electrical Engineering.*

*New set of Boards of Studies, Academic council and Governing Body has further strengthened our hands by endorsing the practices and suggested recommendations.*

*The encouragement given by the affiliating JNTU-K has left no task insurmountable.*

*Principal*

*MEMBERS ON THE BOARD OF STUDIES  
IN  
ELECTRONICS AND COMMUNICATIONS ENGINEERING*

- Head of the Department.
- Dr. B. Prabhakara Rao, Professor, Dept. of ECE & Director of Foreign Affairs, JNTU-K, Kakinada.
- Dr. R.V.S. Satyanarayana, Professor, Department of E.C.E., S.V.U. College of Engg., Tirupati.
- Sri Abraham Verghese, Scientist 'F', Additional Director, NSTL, Visakhapatnam.
- Dr. Namburi Nageswara Rao, Principal, SITAM, Vizianagaram.
- Dr. K. Rajarajeswari, Professor and Chairman, Board of Studies, Dept. of ECE, Andhra University, Visakhapatnam.
- Sri P. Nagaraju, General Manager, BSNL, Visakhapatnam.
- Sri M. Bhuvan Kiran, Management Trainee, Vizag Steel Plant, Visakhapatnam.

All faculty of the department.

**ACADEMIC REGULATIONS**  
(Effective for the students admitted into  
first year from the academic year 2012-2013)

The M.Tech Degree of JNTU-KAKINADA shall be recommended to be conferred on candidates who are admitted to the program and fulfill all the requirements for the award of the Degree.

**1.0 ELIGIBILITY FOR ADMISSION:**

Admission to the above program shall be made subject to the eligibility, qualifications and specialization as per the guidelines prescribed by the APSCHE and AICTE from time to time.

**2.0 AWARD OF M.TECH. DEGREE:**

- a. A student shall be declared eligible for the award of the M.Tech. degree, if he pursues a course of study and completes it successfully for not less than two academic years and not more than four academic years.
- b. A student, who fails to fulfill all the academic requirements for the award of the Degree within four academic years from the year of his admission, shall forfeit his seat in M.Tech. Course.
- c. The duration of each semester will normally be 20 weeks with 5 days a week. A working day shall have 7 periods each of 50minutes.

### 3.0 COURSES OF STUDY:

M.TECH. COURSES	INTAKE
Chemical Engineering	18
Computer Science and Engineering	18
CAD/CAM	18
Infrastructural Engineering and Management	18
Structural Engineering	18
Power System Control and Automation	18
Embedded Systems & VLSI Design	18
Communications & Signal Processing	18
Software Engineering	18
Power Electronics & Drives	18
Computer Aided Analysis And Design (CAAD)	18

### 4.0 ATTENDANCE:

The attendance shall be considered subject wise.

- a. A candidate shall be deemed to have eligibility to write end semester examinations in a subject if he has put in at least 75% of attendance in that subject.
- b. Shortage of attendance up to 10% in any subject (i.e. 65% and above and below 75%) may be condoned by a Committee on genuine and valid reasons on representation by the candidate with supporting evidence.
- c. Shortage of attendance below 65% shall in no case be condoned.
- d. A student who gets less than 65% attendance in a maximum of two subjects in any semester shall not be permitted to take the end- semester examination in which he/she falls short His/her registration for those subjects will be treated as cancelled. The student should re-register and repeat those subjects as and when offered next.



- e. If a student gets less than 65% attendance in more than two subjects in any semester he/she shall be detained and has to repeat the entire semester.
- f. A stipulated fee shall be payable towards condonation of shortage of attendance.

## **5.0 EVALUATION:**

The Performance of the candidate in each semester shall be evaluated subject-wise, with 100 marks for each theory subject and 100 marks for each practical, on the basis of Internal Evaluation and End Semester Examination.

- a. A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.
- b. For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination, 40 marks shall be awarded based on the Internal Evaluation. One part of the internal evaluation shall be made based on the average of the marks secured in the two Mid-Term Examinations of 30 each conducted one in the middle of the Semester and the other immediately after the completion of instruction. Each mid-term examination shall be conducted for a duration of 120 minutes with 4 questions without any choice. The remaining 10 marks are awarded through an average of continuous evaluation of assignments / seminars / any other method, as notified by the teacher at the beginning of the semester.
- c. For Practical subjects, 50 marks shall be awarded based on the performance in the End Semester Examinations, 50 marks shall be awarded based on the day-to-day performance as Internal marks. A candidate has to secure a minimum of 50% in

the external examination and has to secure a minimum of 50% on the aggregate to be declared successful.

- d. There shall be a seminar presentation during III semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee. The Departmental Committee consists of the Head of the Department, supervisor and two other senior faculty members of the department. For Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful.
- e. For Seminar in I, II Semesters in case of the course structure of having 5 Theory + 2 Labs. + 1 Seminar, a student has to deliver a seminar talk in each of the subjects in that semester which shall be evaluated for 10 marks each and average marks allotted shall be considered. A letter grade from A to C corresponding to the marks allotted may be awarded for the two credits so as to keep the existing structure and evaluation undisturbed.

A – Excellent	(average marks > 8)
B – Good	(6 < average marks < 8)
C – Satisfactory	(5 < average marks < 6)

If a satisfactory grade is not secured, one has to repeat in the following semester.

- f. In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.0 a, c) he has to reappear for the End Examination in that subject.

A candidate shall be given one chance to re-register for each

subject provided the internal marks secured by a candidate are less than 50% and he has failed in the subject(s). In such a case the candidate must re-register for the subject (s) and secure required minimum attendance. Attendance in the re-registered subject (s) has to be calculated separately to become eligible to write the end- examination in the re-registered subject(s). In the event of re-registration, the internal marks and end examination marks obtained in the previous attempt are nullified.

- g. In case the candidates secure less than the required attendance in any subject(s), he shall not be permitted to appear for the End Examination in that subject(s). He shall re-register for the subject(s) when next offered.
- h. Laboratory examination for M.Tech subjects must be conducted with two Examiners, one of them being Laboratory Class Teacher and second examiner shall be other than Laboratory Teacher.

## **6.0 EVALUATION OF PROJECT / DISSERTATION WORK:**

Every candidate shall be required to submit the thesis or dissertation after taking up a topic approved by the Departmental Research Committee (DRC).

- a. A Departmental Research Committee (DRC) shall be constituted with the Head of the Department as the chairman and two senior faculty as members to oversee the proceedings of the project work from allotment to submission.
- b. A Central Research Committee (CRC) shall be constituted with a Senior Professor as chair person, Heads of all the Departments which are offering the M.Tech. programmes and two other senior faculty members.
- c. Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance

- requirement of all the subjects (theory and practical subjects.)
- d. After satisfying 6.0 c, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the DRC for its approval. Only after obtaining the approval of DRC the student can initiate the Project work
  - e. If a candidate wishes to change his supervisor or topic of the project he can do so with approval of DRC. However, the Departmental Project Review Committee shall examine whether the change of topic/supervisor leads to a major change in his initial plans of project proposal. If so, his date of registration for the Project work shall start from the date of change of Supervisor or topic as the case may be whichever is earlier.
  - f. A candidate shall submit and present the status report in two stages at least with a gap of 3 months between them after satisfying 6.0 d.
  - g. The work on the project shall be initiated in the beginning of the second year and the duration of the project is for two semesters. A candidate shall be permitted to submit his dissertation only after successful completion of all theory and practical subject with the approval of CRC but not earlier than 40 weeks from the date of registration of the project work. For the approval by CRC the candidate shall submit the draft copy of the thesis to the Principal through the concerned Head of the Department and shall make an oral presentation before the CRC.
  - h. Three copies of the dissertation certified by the supervisor shall be submitted to the College after approval by the CRC.
  - i. The dissertation shall be adjudicated by one examiner selected by the Principal. For this HOD shall submit in consultation with the supervisor a panel of 5 examiners, who are experienced in that field.

- j. If the report of the examiner is not favorable, the candidate shall revise and resubmit the dissertation, in a time frame as prescribed by the CRC. If the report of the examiner is unfavorable again, the dissertation shall be summarily rejected then the candidate shall change the topic of the Project and option shall be given to change the supervisor also.
- k. If the report of the examiner is favorable, viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the Department and the examiner who adjudicated the dissertation. The Board shall jointly report candidate's work as:
  - A. Excellent
  - B. Good
  - C. Satisfactory

**7.0 AWARD OF DEGREE AND CLASS :**

A candidate shall be eligible for the respective degree if he satisfies the minimum academic requirements in every subject and secures satisfactory or higher grade report on his dissertation and viva-voce.

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M.Tech. Degree he shall be placed in one of the following three classes.

<b>% of Marks secured</b>	<b>Class Awarded</b>
70% and above	First Class with Distinction
60% and above but less than 70%	First Class
50% and above but less than 60%	Second Class

The marks in internal evaluation and end examination shall be shown separately in the marks memorandum.

The grade of the dissertation shall also be mentioned in the marks memorandum.

## **8.0 WITHHOLDING OF RESULTS:**

If the candidate has not paid any dues to the college or if any case of indiscipline is pending against him, the result of the candidate will be withheld and he will not be allowed into the next higher semester. The recommendation for the issue of the degree shall be liable to be withheld in such cases.

## **9.0 TRANSITORY REGULATIONS:**

A candidate who has discontinued or has been detained for want of attendance or who has failed after having studied the subject is eligible for admission to the same or equivalent subject(s) as and when subject(s) is/are offered, subject to 6.0 e and 2.0

## **10.0 GENERAL**

1. The academic regulations should be read as a whole for purpose of any interpretation.
2. In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman Academic Council is final
3. The College may change or amend the academic regulations and syllabus at any time and the changes amendments made shall be applicable to all the students with effect from the date notified by the College.
4. Wherever the word he, him or his occur, it will also include she, hers.

## COURSE STRUCTURE

### I SEMESTER

<b>COURSE CODE</b>	<b>THEORY/LAB</b>	<b>L</b>	<b>P</b>	<b>C</b>
10EC2101	Embedded System Concepts	4	-	4
10EC2102	VLSI Technology & Design	4	-	4
10EC2103	Digital Design through HDL	4	-	4
10EC2104	Digital Signal Processing	4	-	4
10EC2105	Microcontroller Applications	4	-	4
	Elective I	4		4
			-	
10EC2106	Digital Data Communications			
10EC2107	CPLD and FPGA Architecture and Applications			
10EC2108	System Modelling and Simulation			
10EC2109	HDL Programming Lab		3	2
<b>Total</b>		<b>24</b>	<b>3</b>	<b>26</b>

### II SEMESTER

<b>COURSE CODE</b>	<b>THEORY/LAB</b>	<b>L</b>	<b>P</b>	<b>C</b>
10EC2110	Embedded Computing Systems	4	-	4
10EC2111	Analog IC Design	4	-	4
10EC2112	Low Power VLSI Design	4	-	4
10EC2113	DSP Processors and Architecture	4	-	4
10EC2114	Digital Systems Design	4	-	4
	Elective-II	4	-	4
10EC2115	Electronic Design Automation Tools			
10EC2116	Image Processing			
10EC2117	Computer Networks			
10EC2118	Embedded Systems Lab	-	3	2
<b>Total</b>		<b>24</b>	<b>3</b>	<b>26</b>

**III SEMESTER**

<b>COURSE CODE</b>	<b>THEORY/LAB</b>	<b>L</b>	<b>P</b>	<b>C</b>
<i>Commencement of Project Work</i>				
10EC21S1	SEMINAR	-	-	<b>2</b>

**IV SEMESTER**

<b>COURSE CODE</b>	<b>THEORY/LAB</b>	<b>L</b>	<b>P</b>	<b>C</b>
10EC2119	PROJECT WORK DISSERTATION / THESIS EXCELLENT/GOOD/SATISFACTORY/ NON-SATISFACTORY	-	-	<b>56</b>



**EMBEDDED SYSTEM CONCEPTS****Course Code: 10EC2101****L P C**  
**4 0 4****UNIT- I****Introduction to Embedded Systems**

Embedded system, processor in the system, other hardware units, software embedded into a system, exemplary embedded systems, embedded system – on – chip (SOC) and in VLSI circuit.

**UNIT- II****Processor and Memory Organization**

Structural units in a Processor, Processor selection for an embedded system, memory devices, memory selection for an embedded system, allocation of memory to program segments and blocks and memory map of a system, DMA, interfacing processor, memories and Input Output Devices.

**UNIT- III****Devices and Buses for Device Networks**

I/O devices, timer and counting devices, serial communication using the 'I2 C', CAN and advanced I/O buses between the networked multiple devices, host systems or computer parallel communication between the networked I/O multiple devices using the ISA, PCI, PCI-X and advanced buses.

**UNIT- IV****Device Drivers and Interrupts Servicing Mechanism**

Device drivers, parallel port and serial port device drivers in a system, device drivers for internal programmable timing devices, interrupt servicing mechanism.

## **UNIT- V**

### **Programming Concepts and Embedded Programming in C and C++**

Software programming in assembly language(ALP) and in high level language 'C','C' program elements: header and source files and preprocessor directives, program elements: macros and functions, data types ,data structures, modifiers , statements , loop and pointers, queues ,stacks , lists and ordered lists, embedded programming in C++, embedded programming in java,'C' program compiler and cross-compiler , source code engineering tools for embedded C/C++,optimization of memory needs.

## **UNIT- VI**

### **Program Modelling Concepts in Single and Multi Processor Systems Software - Development Process**

Modeling processes for software analysis before software implementation, programming models for event controlled or response time constrained real time programs, modeling of multi processor systems.

## **UNIT- VII**

### **Hardware and Software Co Design - I**

Embedded System project development, embedded System design and co-design issues in system development process, design cycle in the development phase for an Embedded System.

## **UNIT- VIII**

### **Hardware and Software Co Design – II**

Use of target system or its Emulator and In-Circuit Emulator (ICE), use of Software tools for Development of an Embedded System, use of scopes and logic analyzers for System Hardware Tests

### **Text Book:**

1. Rajkamal, "Embedded systems: Architecture, programming and design", TMH, 2<sup>nd</sup> Edition, 2007.

**References:**

1. Arnold S Burger, “Embedded system Design”, CMP books, 2010.
2. David Simon, “An embedded software primer”, PEA, 2008.
3. Steve Heath, “Embedded systems Design”, ELSEVIER, 2<sup>nd</sup> Edition 2005.

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**VLSI TECHNOLOGY & DESIGN****Course Code : 10EC2102****L P C**  
**4 0 4****UNIT-I****Introduction to MOS Technologies**

Review of Microelectronics, MOS, CMOS, Bi CMOS Technology trends and projections.

**UNIT- II****Basic Electrical Properties of MOS, CMOS & Bi-CMOS Circuits**

$I_{ds}$ - $V_{ds}$  relationships, Threshold voltage  $V_t$ , ' $g_m$ ,  $g_{ds}$  and  $w_o$ ,' Pass Transistor, MOS, CMOS & Bi CMOS Inverters,  $Z_{pu}/Z_{pd}$ , MOS Transistor circuit model, Latch-up in CMOS circuits.

**UNIT- III****Layout Design and Tools**

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

**UNIT- IV****Logic Gates & Layouts**

Static complementary gates, switch logic, Alternative gate circuits, low power gates, Resistive and Inductive interconnect delays.

**UNIT- V****Combinational Logic Networks**

Layouts, Simulation, Network delay, interconnect design, power optimization, Switch logic networks, Gate and Network testing.

## **UNIT- VI**

### **Sequential Systems**

Memory cells and Arrays, clocking disciplines, Design, power optimization, Design validation and testing.

## **UNIT- VII**

### **Floor Planning & Architecture Design**

Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing..

## **UNIT- VIII**

### **Introduction to Cad Systems (Algorithms) and Chip Design**

Layout Synthesis and Analysis, Scheduling and printing; Hardware/Software Co-design, chip design methodologies-Design examples.

## **Text Books**

1. K. Eshraghian, “Essentials of VLSI Circuits and Systems”, PHI 3<sup>rd</sup> Edition, 2005.
2. Wayne Wolf, “Modern VLSI Design”, Pearson Education, 5<sup>th</sup> Indian Reprint, 2005.

## **References**

1. N.H.E Weste, K.Eshraghian, “Principals of CMOS Design”, Adison Wesley, 2<sup>nd</sup> Edition, 2010.
2. Fabricius, “Introduction to VLSI Design”, MGH International Edition, 1990.
3. Baker, Li Boyce, CMOS Circuit Design, Layout and Simulation, PHI, 2004.

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**DIGITAL DESIGN THROUGH HDL****Course Code: 10EC2103****L P C**  
**4 0 4****UNIT- I****The VHDL Design Element**

Structural design elements, data flow design elements, behavioral design elements, time dimension and simulation synthesis.

**UNIT- II****Combinational and Sequential Logic Design (Using VHDL)**

Decoders, encoders, three state devices, multiplexers and demultiplexers, Code Converters, EX-OR gates and parity circuits, comparators, adders & subtractors, ALUs, Combinational multipliers. VHDL codes for the above ICs Barrel shifter, comparators, floating-point encoder, dual priority encoder, Latches and flip-flops, PLDs, counters, shift register and their VHDL models, synchronous design methodology, impediments to synchronous design.

**UNIT- III****Introduction to Verilog**

Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches.

**Language Constructs and Conventions**

Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

## **UNIT- IV**

### **Gate Level Modeling**

Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip-flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits.

## **UNIT- V**

### **Behavioral Modeling**

Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Examples, Assignments with Delays, Wait construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non blocking Assignments, The case statement, Simulation Flow, *if* and *if-else* constructs, assign-deassign construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

## **UNIT- VI**

### **Modeling at Data Flow Level**

Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators.

### **Switch Level Modeling**

Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets, Exercises.

## **UNIT- VII**

### **System Tasks, Functions, and Compiler Directives**

Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations, Exercises.

### **Functions, Tasks, and User-Defined Primitives**

Introduction, Function, Tasks, User- Defined Primitives (UDP), FSM Design (Moore and Mealy Machines).

## **UNIT- VIII**

### **Digital Design With Sm Charts**

State Machine Charts, Derivation of SM Charts, Realization of SM Charts.

#### **Text Books**

1. John F.Wakerly, “Digital Design Principles &Practices”, PHI/Pearson Education, 3<sup>rd</sup> Ed., 2005.
2. T.R.Padmanabhan and B.Bala Tripura Sundari, “Design through Verilog HDL”, WSE, IEEE Press, 2004.

#### **References:**

1. J.Bhasker, “VHDL Primer”, PHI, 3rd Edition,1999.
2. Michael D.Ciletti, “Advanced Digital Design with Verilog HDL”, PHI, 2<sup>nd</sup> Edition, 2005.
3. Samir palmitkar, “Verilog HDL”, 2dn Edition, 2003.
4. J.Bhasker, “A verilog HDL primer”, SG Press, 2<sup>nd</sup> edition, 1997.

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**DIGITAL SIGNAL PROCESSING****Course Code: 10EC2104****L P C**  
**4 0 4****UNIT- I****Introduction**

Introduction to Digital Signal Processing: Discrete time signals & sequences, linear shift invariant systems, stability, and causality. Linear constant coefficient difference equations. Frequency domain representation of discrete time signals and systems.

**UNIT- II****Discrete Fourier Series**

Properties of discrete Fourier series, DFS representation of periodic sequences, Discrete Fourier transforms: Properties of DFT, linear convolution of sequences using DFT, Computation of DFT. Relation between Z-transform and DFS.

**UNIT- III****Fast Fourier Transforms**

Fast Fourier transforms (FFT) - Radix-2 decimation in time and decimation in frequency FFT Algorithms, Inverse FFT, and FFT for composite N.

**UNIT- IV****Realization of Digital Filters**

Review of Z-transforms, Applications of Z – transforms, solution of difference equations of digital filters, Block diagram representation of linear constant-coefficient difference equations, Basic structures of IIR systems, Transposed forms, Basic structures of FIR systems, System function.

## **UNIT- V**

### **IIR digital filters**

Analog filter approximations – Butter worth and Chebyshev, Design of IIR Digital filters from analog filters, Design Examples: Analog-Digital transformations.

## **UNIT- VI**

### **FIR digital filters**

Characteristics of FIR Digital Filters, frequency response, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR & FIR filters.

## **UNIT- VII**

### **Multirate Digital Signal Processing**

Decimation, interpolation, sampling rate conversion, Implementation of sampling rate conversion.

## **UNIT- VIII**

### **Introduction to Dsp Processors**

Introduction to programmable DSPs: Multiplier and Multiplier Accumulator (MAC), Modified Bus Structures and Memory Access schemes in DSPs Multiple access memory, multiport memory, VLSI Architecture, Pipelining, Special addressing modes, On-Chip Peripherals. Architecture of TMS 320C5X- Introduction, Bus Structure, Central Arithmetic Logic UNIT-, Auxiliary Registrar, Index Registrar, Auxiliary Register Compare Register, Block Move Address Register, Parallel Logic Unit, Memory mapped registers, program controller, Some flags in the status registers, On- chip registers, On-chip peripherals.

### **Text Books**

1. John G. Proakis, Dimitris G. Manolakis, “Digital Signal Processing”, Principles, Algorithms, and Applications; Pearson Education / PHI, 2<sup>nd</sup> Edition, 2007.
2. A.V.Oppenheim and R.W. Schaffer, “Discrete Time Signal Processing”, PHI. 2<sup>nd</sup> Edition, 1999.

3. B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, Programming and Applications”, TATA McGraw Hill, 4<sup>th</sup> Reprint Edition, 2002.

**Reference Books:**

1. Andreas Antoniou, “Digital Signal Processing”, TATA McGraw Hill , 2<sup>nd</sup> Reprint Edition, 2006.
2. MH Hayes, Schaum’s Outlines, “Digital Signal Processing”, TATA McGraw Hill, 2<sup>nd</sup> Edition. 2007.
3. TATA McGraw Hill, “DSP Primer” - C. Britton Rorabaugh, , 2<sup>nd</sup> Edition 2005,
4. Robert J.Schilling, Sandra L. Harris, Thomson, “Fundamentals of Digital Signal Processing using Matlab” 2<sup>nd</sup> Edition, 2007.
5. Alan V. Oppenheim, Ronald W. Schaffer, ”Digital Signal Processing”, PHI Ed., 2006.
6. S.K.Mithra, “Digital Signal Processing” 4<sup>th</sup> Edition, TMH,2010.

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**MICROCONTROLLER AND APPLICATIONS****Course Code: 10EC2105****L P C**  
**4 0 4****UNIT- I****Overview of Architecture and microcontroller Resources**

Architecture of a microcontroller – Microcontroller resources – Resources in advanced and next generation microcontrollers – 8051 microcontroller – Internal and External memories – Counters and Timers – Synchronous serial-cum-asynchronous serial communication - Interrupts.

**UNIT- II****8051 Family Microcontrollers Instruction Set**

Basic assembly language programming – Data transfer instructions – Data and Bit manipulation instructions – Arithmetic instructions – Instructions for Logical operations on the ‘Bytes’ among the Registers, Internal RAM, and SFRs – Program flow control instructions – Interrupt control flow.

**UNIT- III****Real Time Control**

Interrupt handling structure of an MCU – Interrupt Latency and Interrupt deadline – Multiple sources of the interrupts – Non-maskable interrupt sources – Enabling or Disabling of the sources – Polling to determine the Interrupt source and assignment of the priorities among them – Interrupt structure in Intel 8051.

**UNIT- IV****Real Time Control Timers**

Programmable Timers in the MCUs – Free running counter and real time control – Interrupt interval and density constraints.

## **UNIT- V**

### **Systems Design**

Digital and Analog Interfacing Methods, Switch, Keypad and Keyboard interfacing – LED and Array of LEDs – Display Systems and its interfaces – Printer interfaces – Programmable instruments interface using IEEE 488 Bus – Interfacing with the Flash Memory – Interfaces – Interfacing to High Power Devices – Analog input interfacing – Analog output interfacing.

## **UNIT- VI**

### **Arm 32 Bit MCUs**

Introduction to 16/32 Bit processors – ARM architecture and organization – ARM / Thumb programming model – ARM / Thumb instruction set – Development tools.

## **UNIT- VII**

### **Real Time Operating System for Micro Controllers**

Real Time operating system – RTOS of Keil (RTX51) – Use of RTOS in Design – Software development tools for Microcontrollers.

## **UNIT- VIII**

### **Microcontroller Based Industrial Applications**

Optical motor shaft encoders – Industrial control – Industrial process control system – Prototype MCU based Measuring instruments – Robotics and Embedded control – Digital Signal Processing and Digital Filters.

### **Text Books**

1. Raj Kamal, “Microcontrollers Architecture, Programming Interfacing and System Design”, Pearson Education, 2005, 2<sup>nd</sup> Edition
2. Mazidi and Mazidi, “The 8051 Microcontroller and Embedded Systems”, PHI, 2000, 4<sup>th</sup> impression.

## Reference Books

1. A.V. Deshmuk, “Microcontrollers (Theory & Applications)”–, TMH, 6<sup>th</sup> Reprint, 2007.
2. John B. Peatman, “Design with PIC Microcontrollers”, Pearson Education, 2005, 2<sup>nd</sup> Edition.

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**DIGITAL DATA COMMUNICATIONS****Course Code: 10EC2106****L P C**  
**4 0 4****UNIT- I****Digital Modulation Techniques**

FSK, MSK, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK Methods, Bandwidth efficiency, Carrier recovery, Clock recovery.

**UNIT- II****Data Communication Methods**

Data Communication Circuit, point-to-point, Multi-point configurations and Topologies, transmission modes, 2-wire and 4-wire operations, Codes, Error detection methods, Error correction methods, Character synchronization.

**UNIT- III****Data Communication Protocols**

Asynchronous protocols, Synchronous protocols, Bisync Protocol, SDLC, HDLC-Frame format, Flow control and error control.

**UNIT- IV****Switching Techniques**

Circuit Switching, Message Switching and Packet Switching principles, Virtual circuit and datagram techniques, X.25 and frame relay.

**UNIT- V****Line Protocols and Congestion Control**

Line protocols: Basic mode, Half-duplex point-to-point protocol, Half-Duplex Multi-Point Protocol, Full-Duplex Protocols, Polling, Roll Call and Hub Polling, Traffic management, Congestion control in packet switching networks and Frame relay.

## **UNIT- VI**

### **Digital Multiplexing-I**

TDM, T1 carrier system, CCITT-TDM carrier system, CODEC chips, Digital hierarchy, Line Encoding, Frame Synchronization.

## **UNIT- VII**

### **Digital Multiplexing - II**

Multiplexers, Statistical multiplexer, Concentrator, front-end communication processor, Digital PBX, long haul communication with FDM, Hybrid data.

## **UNIT- VIII**

### **Optical Communication**

Basic Optical Network Topologies and their performances, SONET/SDH – Transmission formats and Speeds, Optical interfaces, SONET/SDH rings and networks.

### **Text Books:**

1. W. TOMASI: Advanced Electronic Communications Systems, PHI, 6<sup>th</sup> Edition 2004.
2. William Stallings “Data and Computer Communications” , 7/e, PEI.
3. B.Gerd Keiser, “Optical Communications”, PHI 4<sup>th</sup> Edition, 2008.

### **References**

1. T. HOUSELY: Data Communications and Teleprocessing Systems, PHI. 2<sup>nd</sup> Edition, 1987
2. B.A.Forouzon, “Data and Computer Networking Communications”, 3rd TMH, 2010.

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## **CPLD AND FPGA ARCHITECTURE AND APPLICATIONS**

**Course Code: 10EC2107**

**L P C**  
**4 0 4**

### **UNIT- I**

#### **Programmable Logic**

ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic – 10000 series CPLD, AMD's – CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice PLST's Architectures – 3000 Series – Speed Performance and in system programmability.

### **UNIT- II**

#### **FPGAs**

Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs

### **UNIT- III**

#### **Case Studies**

Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and their speed performance.

### **UNIT- IV**

#### **Finite State Machines (FSM) - I**

Top Down Design – State Transition Table, state assignments for FPGAs. Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL.

## **UNIT- V**

### **Finite State Machines (FSM) - II**

Alternative realization for state machine chart using microprogramming. Linked state machines. One – Hot state machine, Petrinetes for state machines – basic concepts, properties, Extended petrinetes for parallel controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

## **UNIT- VI**

### **Fsm Architectures and Systems Level Design**

Architectures centered around non-registered PLDs. State machine designs centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. K Application of One – Hot method. System level design – controller, data path and functional partition.

## **UNIT- VII**

### **Digital Front End Digital Design Tools for (FPGAs & ASICs)**

Using Cadence EDA Tool (“FPGA Advantage”) – Design Flow Using FPGAs

## **UNIT- VIII**

### **Guidelines and Case Studies**

Parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

### **Text Books:**

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, prentice Hall (Pte), 1994.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publications, 1994.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, Reprint 2008.

4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Publications, 1992, 2<sup>nd</sup> Edition.

**Reference:**

1. Richard Flinder , “Engineering Digital Design “, 2<sup>nd</sup> Edition, Academic press.

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**SYSTEM MODELLING & SIMULATION****Course Code : 10EC2108****L P C**  
**4 0 4****UNIT- I**

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

**UNIT- II****Simulation Software**

Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

**UNIT- III****Building Simulation Models**

Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

**UNIT- IV****Modeling Time Driven Systems**

Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.

**UNIT- V****Exogenous Signals and Events**

Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation.

## **UNIT- VI**

### **Markov Process**

Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous-Time Markov processes.

## **UNIT- VII**

### **Event Driven Models**

Simulation diagrams, Queing theory, simulating queing systems, Types of Queues, Multiple servers.

## **UNIT- VIII**

### **System Optimization**

System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation methodology.

### **Text Books:**

1. Frank L. Severance, “System Modeling & Simulation, An Introduction”, –John Wiley & Sons, Reprint 2009.
2. Averill M. Law, W. David Kelton, “Simulation Modelling and Analysis”, TMH, 3<sup>rd</sup> Edition, 2003.

### **Reference Books:**

1. Geoffery Gordon, “Systems Simulation”, PHI, 1978, 2<sup>nd</sup> Edition.

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**HDL PROGRAMMING LAB****Course Code : 10EC2109****L P C**  
**0 3 2**

1. Digital Circuits Description using Verilog and VHDL
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

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**EMBEDDED COMPUTING SYSTEMS****Course Code: 10EC2110**

<b>L</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

**UNIT- I****Introduction to Software Design**

Requirements, specifications, structural and behavioral descriptions, UML.

**UNIT- II****Embedded Processors**

RISC, super scalar, and VLIW architectures, ARM and SHARC, Processor and memory organization and Instruction level parallelism; CPU architectures: Input/output, interrupts, modes, cache memories

**UNIT- III****Embedded Bus Architectures**

Bus architectures and transactions, Serial interconnects, Networked embedded systems: Bus protocols, I2C bus and CAN bus; Internet-Enabled Systems, Design Example-Elevator Controller.

**UNIT- IV****Program Design and Analysis**

Compilers and optimization, Testing, Performance Analysis.

**UNIT- V****Operating Systems**

Tasks, context switches, Operating system support (inter-process communication, networking), Scheduling, Development environment.

**UNIT- VI****Hardware Accelerators**

FPGA architectures, RISC IP Cores, Verilog HDL.

## **UNIT- VII**

### **Embedded System Application**

Design challenge – optimizing design metrics, processor technology, design technology; real time-operating system: system modeling, static scheduling, Priority drive scheduling, Synchronization & mutual exclusion (real-time and non-real-time); H/W and S/W co-design; embedded multiprocessor

## **UNIT- VIII**

### **DSP Algorithm Design**

A/D conversion and finite precision analysis, Algorithms for embedded systems: source and channel processing, Portable embedded code. Low Power architectures for embedded systems

### **Text Books:**

1. W. Wolf, Computers as Components: Principles of Embedded Computer System Design, Second Edition, Elsevier/MK, 2005
2. F.Vahid and T.Givargis, Embedded System Design: A Unified Hardware / Software Introduction, Wiley, 2002, 3<sup>rd</sup> Edition

### **Reference Books:**

- 1 P.Marwedel, Embedded System Design, Springer, 2006, 2nd Edition
2. Proceedings of the IEEE (Special Issue on HW/SW Codesign), March, 1997.

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**ANALOG IC DESIGN****Course Code: 10EC2111****L P C**  
**4 0 4****UNIT- I****Integrated Devices and Modeling and Current Mirror**

Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT

**UNIT- II****Basic Current Mirrors and Single Stage Amplifiers**

Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load .Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors And Bipolar Gain Stages, Frequency Response.

**UNIT- III****Operational Amplifier Design and Compensation**

Two Stage CMOS Operational Amplifier, Feedback and Operational Amplifier Compensation.

**UNIT- IV****Advanced Current Mirrors and Opamps**

Advanced Current Mirror, Folded – Cascode Operational Amplifier, Current Mirror Operational Amplifier, Fully Differential Operational Amplifier. Common Mode Feedback Circuits, Current Feedback Operational Amplifier, Comparator, Charge Injection Error, Latched Comparator and Bi CMOS Comparators.

**UNIT- V****Sample and Hold & Switched Capacitor Circuits**

MOS, CMOS, BiCMOS Sample and Hold Circuits, Switched Capacitor Circuits: Basic Operation and Analysis, First Order and Biquard Filters,

Charge Injection, Switched Capacitor Gain Circuit, Correlated Double Sampling Techniques. Other Switched Capacitor Circuits.

## **UNIT- VI**

### **Data Converters**

Ideal D/A & A/D Converters, Quantization Noise, Performance Limitations, Nyquist Rate D/A Converters: Decoder Based Converters, Binary Scaled Converters, Hybrid Converters.

## **UNIT- VII**

### **Nyquist Rate A/D Converters**

Nyquist Rate A/D Converters: Integrating, Successive Approximation, Cyclic, Flash Type, Two Step, Interpolating, Folding and Pipelined A/D Converters.

## **UNIT- VIII**

### **Over Sampling Converters and Filters**

Over Sampling with and Without Noise Shaping, Digital Decimation Filter, High Order Modulators, Band Pass Over Sampling Converter, Practical Considerations, Continuous Time Filters.

### **Text Book:**

- 1.D.A.JOHN & KEN MARTIN: Analog Integrated Circuit Design. John Wiley, Reprint 2008.

### **Reference Book:**

1. GREGOLIAN & TEMES: Analog MOS Integrated Circuits, John Wiley, 1986.
2. Paul R.Gray.et.al, Analysis and Design of Analog Integrated circuits, John Wiley reprint, 4<sup>th</sup> edition, 2009.
- 3.Behzad Razavi, Design of Analog CMOs Integrated circuits, Tata Mc Graw Hill Edition, reprint, 2008.

**LOW POWER VLSI DESIGN****Course Code: 10EC2112****L P C**  
**4 0 4****UNIT- I****Low Power Design, an Over View**

Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

**UNIT- II****MOS/Bi-CMOS Processes**

Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

**UNIT- III****Low-Voltage/Low Power MOS/BiCMOS Processes**

Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

**UNIT- IV****Device Behavior and Modeling**

Advanced MOSFET models, limitations of MOSFET models, Bipolar models.

**UNIT- V**

Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

**UNIT- VI****CMOS and Bi-CMOS Logic Gates**

Conventional CMOS and BiCMOS logic gates, Performance evaluation.

## **UNIT- VII**

### **Low- Voltage Low Power Logic Circuits**

Comparison of advanced BiCMOS Digital circuits, ESD-free BiCMOS, Digital circuit operation and comparative Evaluation.

## **UNIT- VIII**

### **Low Power Latches and Flip Flops**

Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

### **Text Book:**

1. Low power by Yeo Rofail/Gohl(3 Authors), “CMOS/Bi CMOS ULSI Low Voltage”, -Pearson Education Asia 1<sup>st</sup> Indian reprint,2002.

### **References :**

1. J.Rabaey, “Digital Integrated circuits”, PH. N.J 1996, 2<sup>nd</sup> Edition
2. Sung-mokang and yusuf leblebici, “CMOS Digital ICs”, TMH , 3<sup>rd</sup> edition , 2003.
3. Parhi, “VLSI DSP Systems”, John Wiley & sons, 2003 Reprint
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

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## DSP PROCESSORS AND ARCHITECTURE

**Course Code: 10EC2113**

**L P C**  
**4 0 4**

### **UNIT- I**

#### **Introduction to Digital Signal Processing**

Introduction, Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

### **UNIT- II**

#### **Computational Accuracy in DSP Implementations**

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

### **UNIT- III**

#### **Architectures for Programmable DSP Devices**

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

### **UNIT IV**

#### **Execution Control and Pipelining**

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

## **UNIT- V**

### **Programmable Digital Signal Processors**

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

## **UNIT- VI**

### **Implementations of Basic DSP Algorithms**

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

## **UNIT- VII**

### **Implementation of FFT Algorithms**

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

## **UNIT- VIII**

### **Interfacing Memory and I/O Peripherals to Programmable DSP Devices**

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

### **Text Books:**

1. Avtar Singh and S. Srinivasan, “Digital Signal Processing” Thomson Publications, 2004.
2. Lapsley et al “DSP Processor Fundamentals, Architectures & Features” S.Chand & Co, 2000, Reprint.

### **References:**

1. B. Venkata Ramani and M. Bhaskar, “Digital Signal Processors, Architecture, Programming and Applications” TMH, 4<sup>th</sup> Reprint,2008.
2. Jonatha Stein, “Digital Signal Processing” , John Wiley, 2005.

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**DIGITAL SYSTEM DESIGN**

	<b>L</b>	<b>P</b>	<b>C</b>
<b>Course Code: 10EC2114</b>	<b>4</b>	<b>0</b>	<b>4</b>

**UNIT– I****Design of Digital Systems**

ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

**UNIT– II****Sequential Circuit Design**

Design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

**UNIT– III****Fault Modeling**

Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults.

**Test Generation**

Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

**UNIT – IV****Test Pattern Generation**

D – algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

**UNIT – V****Fault Diagnosis in Sequential Circuits**

State identification and fault detection experiment. Machine identification, Design of fault detection experiment.



## **UNIT – VI**

### **Programming Logic Arrays**

Design using PLA's, PLA minimization and PLA folding.

## **UNIT – VII**

### **PLA Testing**

Fault models, Test generation and Testable PLA design.

## **UNIT – VIII**

### **Asynchronous Sequential Machine**

Fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

## **Text Books**

1. N. N. Biswas, "Logic Design Theory", PHI, 2009.
2. Zvi Kohavi, "Switching and Finite Automata Theory", TMH, 2<sup>nd</sup> Edition, 2005,
3. Norman Balabanian, Bradley Carlson, "Digital Logic Design Principles" Wiley Student Edition, 2007, Reprint.

## **Reference Books**

1. M. Abramovici, Melvin Breuer, Arthur Friedman—"Digital System Testing and Testable Design", Jaico Publications, 2008, Reprint Edition
2. Charles H. Roth Jr. – "Fundamentals of Logic Design", Cengage learning, 2004 6<sup>th</sup> Edition.
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4<sup>th</sup> Edition, 1993.

**ELECTRONIC DESIGN AUTOMATION TOOLS****Course Code: 10EC2115****L P C**  
**4 0 4****UNIT I****Important Concepts in Verilog**

Basics of Verilog Language, Operators, Hierarchy, Procedures and Assignments, Timing Controls and Delay, Tasks And Functions Control Statements, Logic-Gate Modeling, Modeling Delay, Altering Parameters, Other Verilog Features.

**UNIT- II****Simulation Using HDLS I**

Simulation-Types of Simulation, Logic Systems, Working Of Logic Simulation, Cell Models, Delay Models State Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation.

**UNIT- III****Synthesis Using HDLS**

Verilog and Logic Synthesis, VHDL and Logic Synthesis, Memory Synthesis, FSM Synthesis, Memory Synthesis, Performance-Driven Synthesis.

**UNIT- IV****Cad Tools for Simulation and Synthesis**

Modelsim and Leonardo Spectrum (Exemplar).

**UNIT- V****Tools for Circuit Design and Simulation Using PSPICE**

Pspice Models For Transistors, A/D & D/A Sample and Hold Circuits Etc, and Digital System Building Blocks, Design and Analysis Of Analog and Digital Circuits Using PSPICE.

## **UNIT- VI**

### **An Over View of Mixed Signal VLSI Design**

Fundamentals Of Analog and Digital Simulation, Mixed Signal Simulator Configurations, Understanding Modeling, Integration to CAD Environments.

## **UNIT- VII**

### **Analysis of Analog Circuits**

A/D, D/A Converters, Up And Down Converters, Comparators Etc.

## **UNIT- VIII**

### **Tools for PCB Design and Layout**

An Overview Of High Speed PCB Design, Design Entry, Simulation and Layout Tools for PCB, introduction to Orcad PCB Design Tools.

### **Text Books:**

1. J.Bhaskar, A Verilog Primer, BSP, 2003 3rd Edition.
2. J.Bhaskar, A Verilog HDL Synthesis BSP, 2003, 2nd Edition.
3. M.H.RASHID: SPICE FOR Circuits and Electronics Using PSPICE (2/E) (1992) Prentice Hall.

### **References:**

1. ORCAD: Technical Reference Manual, Orcad, USA.
2. SABER: Technical Reference Manual, Analogy Nic, USA.
3. M.J.S.SMITH: Application-Specific Integrated Circuits (1997).  
Addison Wesley
4. J.Bhaskar, A VHDL Synthesis Primer, BSP, 2003, 3rd Edition.

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## IMAGE PROCESSING

**Course Code : 10EC2116**

**L P C**  
**4 0 4**

### **UNIT – I**

#### **Image Processing Fundamentals**

Image Transforms – Fourier Transform, Walsh, Hadamard, DCT, Haar, Slant, KL transforms and their properties.

### **UNIT – II**

#### **Image Enhancement**

Enhancement by point processing, Histogram Processing, Enhancement in Spatial domain and in Frequency domain.

### **UNIT – III**

#### **Color Image Processing**

Fundamentals – Models – Pseudo Color image processing – Basics – Converting to other color spaces – Transformations - Color Smoothing and Sharpening – Color Segmentation – Noise – Color Noise Compression.

### **UNIT – IV**

#### **Image Filtering and Restoration**

Degradation Model – Diagonalisation of Circulant and Block Circulant Matrices – Algebraic approach to restoration- Inverse filtering – LMS Restoration – Constrained least Squares and iterative restoration, Geometric Transformations.

### **UNIT – V**

#### **Image Compression**

Fundamentals – Compression Models – Lossless and Lossy compressions – Compression Standards.

## **UNIT – VI**

### **Image Segmentation**

Detection of discontinuities – Edge linking and boundary detection – Region oriented segmentation – use of motion in segmentation – Marr-Hildreth Edge Detection – Canny Detectors.

## **UNIT – VII**

### **Representation and Description**

Various schemes – Boundary Descriptors – Regional Descriptors.

## **UNIT – VIII**

### **Morphological Image Processing**

Preliminaries – Dilation & Erosion – Opening & Closing – Hit-Miss Transformation – Morphological algorithms – Extension to Grey Scale Images.

### **Text Books:**

1. Rafael C.Gonzalez, Richard E. Woods, “Digital Image Processing”, Pearson education, 2<sup>nd</sup> Edition.
2. Rafael C.Gonzalez, Richard E.Woods, Steven L.Edding, “Digital. Image Processing Using MATLAB”, Pearson Education, 2<sup>nd</sup> Edition

### **References:**

1. AK Jain, “Fundamentals of Digital Image Processing”, PHI.
2. William K Pratt, “Digital Image Processing”, John Wiley, 3<sup>rd</sup> Edition ,2006.
3. Fundamentals of Electronic Image Processing weeks Jr. SPIC/IEEE series PHI

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## COMPUTER NETWORKS

**Course Code: 10EC2117**

**L P C**  
**4 0 4**

### UNIT- I

#### **Introduction**

OSI, TCP/IP and other networks models, Examples of Networks: Novell Networks, Arpanet, Internet, Network Topologies WAN, LAN, MAN.

### UNIT- II

#### **Physical Layer**

Transmission media copper, twisted pair wireless, switching and encoding asynchronous communications; Narrow band, broad band ISDN and ATM.

### UNIT- III

#### **Data Link Layer**

Design issues, framing, error detection and correction, CRC, Elementary Protocol-stop and wait, Sliding Window, Slip, Data link layer in HDLC, Internet, ATM.

### UNIT- IV

#### **Medium Access Sub Layer**

ALOHA, MAC addresses, Carrier sense multiple access, IEEE 802.X Standard Ethernet, wireless LANS, Bridges.

### UNIT- V

#### **Network Layer**

Virtual circuit and Datagram subnets-Routing algorithm shortest path routing, Flooding, Hierarchical routing, Broad cast, Multi cast, distance vector routing.

## **UNIT- VI**

### **Dynamic Routing**

Broadcast routing. Rotary for mobility, Congestion, Control Algorithms – General Principles of Congestion prevention policies. Internetworking: The Network layer in the internet and in the ATM Networks.

## **UNIT- VII**

### **Transport Layer**

Transport Services, Connection management, TCP and UDP protocols; ATM AAL Layer Protocol.

## **UNIT- VIII**

### **Application Layer**

Network Security, Domain name system, SNMP, Electronic Mail; the World WEB, Multi Media.

### **Text Books:**

1. Andrew S Tanenbaum, “Computer Networks” Pearson Education /PHI, 4<sup>th</sup> edition, 2010.
2. Behrouz A. Forouzan “Data Communications and Networking”, TMH, Third Edition

### **References :**

1. S.Keshav, “An Engineering Approach to Computer Networks” Pearson Education , 2nd Edition.
2. W.A. Shay, Thomson, “Understanding communications and Networks”, 3rd Edition.

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**EMBEDDED SYSTEM LAB****Course Code: 10EC2118****L P C**  
**0 3 2**

1. Write an assembly language program for square wave generation using 8051 timers.
2. Write an assembly language program for establishing serial communication using 8051 serial interrupts.
3. Write an assembly language program for interfacing LCD display unit to 8051.
4. Write an assembly language program for interfacing stepper motor to 8051 micro controller.
5. Write an assembly language program for performing arithmetic operation on ARM microcontroller.
6. Write an assembly language program for matrix multiplication on ARM microcontroller.
7. Write an assembly language program for serial communication using ARM microcontroller.

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