SCHEME OF COURSE WORK

Course Details:

Course Title	**: EMBEDDED SYSTEMS**		
Course Code	**: 13EC1133**	**L T P C**	**: 4 0 0 3**
Program:	**: B.Tech.**		
Specialization:	**: Electronics and Communication Engineering**		
Semester	**: VII**		
Prerequisites	**: Digital logic design, computer organization**		
Courses to which it is a prerequisite	**: --**		

Course Outcomes (COs):

1	Describe the concepts of embedded system and desktop system and their technology
2	Explain the General Purpose Processors, ASIP, DSP Processors.
3	Demonstrate advantages of State Machine Models, Communication Protocols and Synchronization techniques
4	Summarize the serial communication interfacing
5	Specify different design Technologies of software and hardware design

Course Outcomes versus Program Outcomes:

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**S**	**S**	**M**	**M**	**M**	**M**						
CO2	**S**	**S**	**S**	**S**	**S**	**M**						**M**
CO3	**S**	**S**	**M**	**M**	**S**							
CO4		**M**	**M**		**M**	**M**						
CO5		**S**	**M**	**M**								**M**

S - Strongly correlated, M - Moderately correlated, Blank - No correlation

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Teaching-Learning and Evaluation

Week	Topic / contents	Course outcomes	Sample questions	Teaching-learning strategy	Assessment method & schedule
1	Embedded systems overview, design challenge, processor technology, IC technology,	CO-1	1.What is an embedded Microprocessor 2.What are the design metrics for an embedded system	▫ Lecture ▫ Discussion	Assignment 1/ Quiz1/ Mid1
2	Design Technology, Trade-offs. Single purpose processors RT-level combinational logic,	CO-1	1. Explain about design technology. 2.What is RT level combinational logic	▫ Lecture ▫ Discussion	Assignment 1/ Quiz1/ Mid1
3	sequential logic (RT-level), custom single purpose processor design (RT-level), optimizing custom single purpose processors	CO-1	1. Explain the optimization technique of custom single purpose processor. 2. Explain sequential logic (RT-level)	▫ Lecture ▫ Discussion ▫ PPT	Assignment 1/ Quiz1/ Mid1
4	Basic architecture, operation, Pipelining, Programmer's view, development environment	CO-2	1. Draw the architecture of General purpose processor. 2. Explain Pipelining.	▫ Lecture ▫ Discussion ▫ PPT	Assignment 1/ Quiz1/ Mid1
5	Application Specific Instruction-Set Processors (ASIPs) – Micro Controllers and Digital Signal Processors.	CO-2	1. Write short note on Digital Signal Processors. 2. Write about Application specific instruction set processors	▫ Lecture ▫ Discussion	Assignment 1/ Quiz1/ Mid1
6	Introduction, Models vs. Languages, finite state machines with data path model(fsmd)	CO-2	1. Differentiate between models and languages. 2.Explain data path model of FSMD	▫ Lecture ▫ Discussion ▫ Program solving	Assignment 1/ Quiz1/ Mid1
7	FSMD using state machines, program state machine model (psm)	CO-3	1. Explain about program state machine model.	▫ Lecture ▫ Discussion ▫ Program solving	Assignment 1/ Quiz1/ Mid1
8	Concurrent process model, concurrent processes Communication among processes, synchronization among processes	CO-3	1. Explain concurrent process models.	▫ Lecture ▫ Program Solving	Assignment 1/ Quiz1/ Mid1
9	**Mid-Test 1**				

10	Concurrent process model implementation, data flow model, real-time systems.	CO-3	1. Define data flow model. 2. Explain real time systems	▫ Lecture ▫ Discussion ▫ PPT	Assignment 2/ Quiz2/ Mid2
11	Need for communication interfaces, RS232 / UART, RS422 / RS485	CO-4	1. What is Peripheral Interfacing? 2. Write short notes on RS 232/UART.	▫ Lecture ▫ Discussion ▫ PPT	Assignment 2/ Quiz2/ Mid2
12	USB, Infrared, IEEE 1394 Firewire.	CO-4	1. What are the features of USB? 2. Explain about Infrared.	▫ Lecture ▫ Discussion ▫ PPT	Assignment 2/ Quiz2/ Mid2
13	Ethernet, IEEE 802.11, Bluetooth.	C0-4	1. Write short notes on Ethernet. 2. Explain Wireless LAN.	▫ Lecture ▫ Discussion ▫ PPT	Assignment 2/ Quiz2/ Mid2
14	Introduction, Automation, Synthesis, Parallel evolution of compilation and synthesis.	CO-5	1.Define Synthesis 2.What is Parallel evolution of compilation and synthesis.	▫ Lecture ▫ Discussion	Assignment 2/ Quiz2/ Mid2
15	Logic Synthesis, RT synthesis, Behavioral Synthesis	CO-5	1. Explain RT Synthesis 2. What is logic synthesis	▫ Lecture ▫ Discussion	Assignment 2/ Quiz2/ Mid2
16	Systems Synthesis and Hardware/ Software Co-Design ,Verification	CO-5	1. What is verification? 2. Describe hardware/ software co-design	▫ Lecture ▫ Discussion	Assignment 2/ Quiz2/ Mid2
17	Hardware/Software co-simulation, Reuse of intellectual property cores	CO-5	1. What is hardware/Softwar co-simulation? 2. Write notes on IP cores.	▫ Lecture ▫ Discussion	Assignment 2/ Quiz2/ Mid2
18	**Mid-Test 2**				
19/20	**END EXAM**				