SCHEME OF COURSE WORK

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Course Details:

Course Title	**: VLSI TECHNOLOGY AND DESIGN**		
Course Code	**: 13EC2202**	**L T P C**	**: 4 0 0 3**
Program:	**:M.Tech (VLSI DESIGN AND EMBEDDED SYSTEMS)**		
Specialization:	**: Electronics and Communication Engineering**		
Semester	**: I SEM**		
Prerequisites	**VLSI Design**		
Courses to which it is a prerequisite	**: LOW POWER VLSI**		

Course Outcomes (COs):

1	Distinguish different IC technologies and analyze basic electrical properties of MOS, CMOS, & BI CMOS circuits
2	Design layouts for logic Circuits
3	Analyze the concepts of alternate gate circuits, interconnect delays, Gate and Network Testing
4	Outline the concepts of memory cells, clocking disciplines, power optimization, design validation and Testing.
5	Acquire knowledge of floor-plan methods, High level synthesis, CAD systems and Methodologies for chip design

Course Outcome Vs **Program Outcomes:**

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**
CO1	**S**	**S**	**S**	**S**	**S**	**S**			**S**		**S**
CO2	**S**	**S**	**S**	**M**	**S**	**S**			**S**		**S**
CO3	**M**	**S**	**S**	**S**	**S**	**S**			**M**		
CO4	**S**	**S**	**S**	**S**	**S**	**S**	**S**		**S**		**S**
CO5	**M**	**M**	**S**	**M**	**S**	**M**			**S**		**S**

S - Strongly correlated, *M* - *Moderately* correlated, *Blank* - *No correlation*

Assessment Methods:	Assignment / Seminar / Case Study / Mid-Test / End Exam

Teaching-Learning and Evaluation

Week	Topic / Contents	Course Outcomes	Sample questions	Teaching-Learning Strategy	Assessment Method & Schedule
1	**Review of Microelectronics**:MOS, CMOS,BICMOS Technology trends and projections	CO-1	1. Explain Masking steps to fabricate a MOS transistor. Explain Masking steps to fabricate a CMOS/ BICMOS transistor.	▫ Lecture ▫ Demo	Mid-I/ Assignment -I
2	Ids-Vds relationships, Threshold voltage V_t,G_m,G_{ds} and W_o	CO-1	1.Derive an expression to give relation between V_{DS}, I_{DS}. 2.Discuss about the threshold voltage in a MOSFET. 3.Explain the dependency of drain current on different material and electrical characteristics.	▫ Lecture Problem solving	Mid-I/ Assignment -I
3	Pass Transistor, MOS,CMOS and BICMOS Inverters,Z_{pu}/Z_{pd}, MOS transistor circuit model, Latch-up in CMOS circuits. **UNIT-2 Layout Design And Tools,** transistor structures, Wires and Vias, Scalable Design Rules	CO-1	1. Write a short note on λ-based design rules. 2. Explain about different contacts and vias.	▫ Lecture	Mid-I/ Assignment -I
4	Layout Diagrams for NMOS and CMOS Inverters and Gates, Layout Design tools Wires and vias	CO-2	Draw the stick and layout for NMOS Inverter, p-well CMOS inverter. 2 a) Write a short note on wires and vias. Explain about the parasitic capacitances.	▫ Lecture	Mid-I/ Assignment -I
5	**UNIT-3 Logic Gates And Combinational Logic Networks,** Static complementary gates, Switch logic, Alternative gate circuits.	CO-3	1. a) Explain about complimentary CMOS gates. Describe about logic levels. b) Draw and explain the logic circuit and stick diagram for	▫ Lecture	Mid-I/ Assignment -I

			F=(A+BC+ABD)' using Complementary CMOS logic.		
6	low power gates ,Resistive and inductive interconnect delays	CO-3	1.a) Discuss the dynamic behavior of CMOS transistor and its capacitances.	▫ Lecture	Mid-I/ Assignment -I
7	Layouts Simulation, Network delay	CO-3	1.a) Write a short note on delay and Transitions. b) Obtain the expression for delay time using RC equivalent of CMOS.	▫ Lecture	Mid-I/ Assignment -I
8	Interconnect design	CO-3	1.Explain the different interconnect delay models and obtain the expression for delay time in each case.	▫ Lecture	Mid-I/ Assignment -I
9	**MID-I**	CO-1 & CO-2			MIDTEST-I
10	Power optimization, Switch logic networks, Gate and network testing	CO-3	1. Explain the methods for optimization of power. What is the method for designing Power networks?	▫ Lecture ▫ Discussion	Mid-2/ Assignment -2
11	**UNIT-4 Sequential Systems** Memory cells and arrays, Clocking disciplines Design, Power optimization	CO-4	1.Explain about the structural specification of sequential machines with state transition graphs and state tables?	▫ Lecture ▫ Discussion	Mid-2/ Assignment -2
12	Design validation and testing	CO-4	1. What are the various methods for testing stuck at faults? 2. Explain the methods for testing faulty gate in a combinational network.	▫ Lecture ▫ Discussion	Mid-2/ Assignment -2
13	**UNIT-5 Floor Planning and Chip Design** Floor planning methods Off-chip connections High-level synthesis	CO-5	1) Briefly explain about floor planning methods.	▫ Lecture ▫ Discussion	Mid-2/ Assignment -2
14	Architecture for low power, SOCs and	CO-5	1.Write a short note on high level synthesis and	▫ Lecture ▫ Discussion	Mid-2/ Assignment -2

	embedded CPUs, Architecture testing,		explain how SOC architectures will be tested?		
15	Introduction to CAD systems(algorithms) and chip design, Layout synthesis and analysis,	CO-5	Describe the Chip design methodology with the help of design flow block diagram.	▫ Lecture ▫ Discussion	Mid-2/ Assignment -2
16	Scheduling and binding, Hardware/software co-design	CO-5	Explain the concept of Hardware/software co-design in VLSI systems.	▫ Lecture ▫ Discussion	Mid-2/ Assignment -2
17	Chip design methodologies-a simple design example. Discussion previous papers, revision, practices.	CO-5	Describe the Chip design methodology with the help of design flow block diagram.	▫ Presentation ▫ Discussion	Mid-2/ Assignment -2
18	**MIDEXAM-II**				MID TERM-II
19/20	**END EXAM**				