SCHEME OF COURSE WORK

Course Title	:VLSI Design		
Course Code	:13EC1117	L T P C	4 1 0 3
Program:	:B.Tech		
Specialization:	: Electronics and Communication Engineering		
Semester	:V		
Prerequisites	: Electronics Devices and Circuits, Switching Theory and Logic Design.		
Courses to which it is a prerequisite	: Digital IC Design		

Course Outcomes (Cos):

1	Distinguish different IC technologies and basic electrical properties of MOS, CMOS and Bi-CMOS circuits.
2	Draw stick diagrams, layout diagrams for logic gates and understand different scaling models.
3	Design subsystem consisting of Combinational and sequential circuits
4	Comprehend CPLD, FPGA architecture and standard cells.
5	Comprehend tools for design and verification.

Course Outcomes versus Program Outcomes:

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**S**	**S**		**S**	**M**							**M**
CO2	**M**	**M**		**S**	**M**							**M**
CO3	**S**	**S**		**S**	**M**							**M**
CO4	**M**	**S**		**M**	**M**							**M**
CO5		**S**		**M**	**S**							**M**

S - Strongly correlated, M - Moderately correlated, Blank - No correlation

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Week	Topic /Contents	Course Outcomes	Sample questions	Teaching-Learning Strategy	Assessment Method & Schedule
1	VLSI Design Flow, Introduction to IC Technology–MOS, PMOS, NMOS	CO1	1. With neat sketches explain NMOS fabrication process? 2. Explain the MOS Transistor operation with the help of neat sketches in Enhancement Mode.	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
2	CMOS & Bi-CMOS technologies.	CO1	1. With neat sketches explain CMOS fabrication in p-well process? 2. With neat sketches explain BICMOS fabrication in an n-well process.	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
3	Basic Electrical Properties of MOS and Bi-CMOS Circuits: I_{ds}-V_{ds} relationships, MOS transistor threshold Voltage, g_m, g_{ds}, figure of merit	CO1	1. Derive an equation for Ids of an n-channel enhancement MOSFET operating in saturation & non-saturation regions. 2. Define figure of merit of MOSFET and deduce the same for a MOSFET when it is biased to operate as a switch.	Lecture/ Problem solving	Assignment I/Quiz-I/Mid-I
4	Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design, Bi-CMOS Inverters.	CO1	1. Determine the pull up to pull down ratio of an NMOS inverter driven through one or more pass transistors. 2. With neat sketches, explain the transfer characteristic of a CMOS inverter. 3. Explain the operation of simple Bi-CMOS inverter and alternative circuits with no static current flow and better output swing.	Lecture/ Problem solving	Assignment I/Quiz-I/Mid-I
5	MOS Layers, Stick Diagrams, Design Rules and Layout, CMOS Design rules for wires, Contacts and Transistors	CO2	1. Explain the design rules for wires, transistors and vias for NMOS & CMOS processes. 2. Design a stick diagram for two-input N-MOS NOR gate.	Lecture/ Design	Assignment I/Quiz-I/Mid-I
6	Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits, Limitations of Scaling.	CO2	1. Design a layout for CMOS 2-input NAND gate. 2. Explain scaling factors for various device parameters.	Lecture/ Design	Assignment I/Quiz-I/Mid-I
7	Basic circuit concepts: Sheet Resistance R_S and its concept to MOS, Area Capacitance Units, Calculations	CO3	1. Explain the concept of sheet resistance and apply it to compute the ON resistance (VDD to GND) of an NMOS inverter having pull up to pull down ratio of 4:1, If n channel resistance is $R_{sn} = 10^4$ per square. 2. Define and explain the following: a. Sheet resistance concept applied to MOS transistors and	Lecture/ Problem solving	Assignment I/Quiz-I/Mid-I

			inverters. b. Standard unit of capacitance.		
8	Delays, Driving large Capacitive Loads.	CO3	1. Explain the following: a. The delay unit. b. Inverter delays. 2. Explain about super buffers.	Lecture/ Problem solving	Assignment I/Quiz-I/Mid-I
9	Mid-Test-1	--	---------	------	----------
10	Wiring Capacitances, Fan-in and fan-out, Choice of layers Transmission Gates, Alternate gate circuits	CO3	1. Explain other forms of CMOS logic. 2. Explain about wiring capacitances.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
11	Shifters, Adders, ALUs	CO3	1. Draw the circuit diagram for 4-by-4 barrel shifter using MOS switches and explain its shifting operation. 2. Draw and explain carry skip adder and discuss how the delay can be reduced.	Lecture/ Design	Assignment II/Quiz-II/Mid-II
12	Multipliers, Parity generators, Comparators	CO3	1. What are the advantages of Wallace tree multiplier? 2. What is serial-parallel multiplier?	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
13	Zero/One Detectors, High Density Memory Elements.	CO3	1. Explain read and write operations of 1-T DRAM cell. 2. Explain the operation of 6-T SRAM.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
14	Standard Cells, Design Approach.	CO4	1. Discuss in detail standard cell design. 2. Distinguish channeled and channel free gate arrays with neat sketches.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
15	FPGAs (Xilinx 4000series), CPLDs (Xilinx 9500series)	CO4	1. Explain Functional Block architecture of XC9500 CPLD. 2. Explain the operation of I/O architecture of XC4000 series FPGA.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
16	Design methods, Design capture tools, Design Verification Tools, CMOS Testing, Need for testing	CO5	1. Explain about Design Capture Tools. 2. Explain about Design Verification Tools.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
17	Test Principles, Design Strategies for test, Chip level Test Techniques, System-level Test Techniques, and Layout Design for Improved Testability.	CO5	1. Explain various design strategies for test. 2. Explain in detail the boundary scan architecture with a neat sketch.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
18	Mid-Test 2	------	----------		
19/20	END EXAM	------	------		