SCHEME OF COURSE WORK

Course Details:

Course Title	: **SYSTEM ON CHIP ARCHITECTURE**		
Course Code	**:** 13EC2206	**L T P C**	**:4 0 0 3**
Program:	**: M.Tech**		
Specialization:	**: VLSI Design and Embedded Systems**		
Semester	**: I**		
Prerequisites	**: System On Chip Architecture**		
Courses to which it is a prerequisite	**: Embedded systems**		

Course Outcomes (COs):

CO1	Comprehend abstraction in Hardware, SOC of ARM Processor
CO2	Evaluate and analyze system on chip RISC Machine, 3and5 stage Pipeline
CO3	Develop programs on ARM Processor
CO4	Explain Memory Hierarchy ARM Interface
CO5	Integrate the Knowledge of ARM for applications of System on Chip

Course Outcome Vs **Program Outcomes:**

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO-1	S	S	S	S	S							S
CO-2	S	S	S	S	S							M
CO-3	S	S	S	S	S							S
CO-4	S	S	S	S	S	M						S
CO-5	S	S	S	S	S	S	M					S

S - Strongly correlated, *M - Moderately* correlated, *Blank - No correlation*

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Teaching-Learning and Evaluation

Week	TOPIC / CONTENTS	Course Outcomes	Sample questions	TEACHING-LEARNING STRATEGY	Assessment Method & Schedule
1	**UNIT-I** **INTODUCTION:** **INTRODUCTION TO PROCESSOR DESIGN**: Abstraction in hardware design, MUO a simple processor, Processor design trade off, Design for low power consumption.	CO-1	1. Explain the necessity of SOC for embedded systems. 2. What are the different techniques implemented in the design of embedded SOC to low power consumption.	▫ Lecture ▫ Discussion	(Week 1- 2)

4	**UNIT-II** **ARM PROCESSOR AS SYSTEM-ON-CHIP:** Acorn RISC Machine – Architecture inheritance –ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM Co-processor interface.	CO-2	1. Describe the architecture of ARM processor as a SOC. 2. What is pipelining, explain how five stage pipeline of ARM is implemented.	▫ Lecture ▫ Discussion	Assignment 1 (Week 3-5)
5	**UNIT-III** **ARM ASSEMBLY LANGUAGE PROGRAMMING:** ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – co-processor instructions. **Architectural Support for High Level Language -** Data types – Abstraction in software design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory.	CO-3	1. Explain different steps for data transfer from one memory location to another memory location. 2. Describe how high level languages are supported by ARM processors.	▫ Lecture ▫ Discussion ▫ NPTEL	(Week 6 - 8)
6	**MID-TEST 1**			▫	(Week 9)
7	**UNIT-IV** **MEMORY HIERARCHY:** Memory size and speed –on chip memory –caches-cache design an example-Memory management **Architectural Support for System Development**-Advanced Microcontroller bus architecture-ARM Memory Interface-ARM Reference Peripheral specification – Hardware System Prototyping tools – Emulator –Debug architecture	CO-4	1. What is caches memory and how it can speed up memory management. 2. What are the design aspects of emulator for debug architecture.	▫ Lecture ▫ Discussion ▫ NPTEL	(Week 10 - 13)
8	**UNIT-V** **ARCHITECTURAL SUPPORT FOR OPERATING SYSTEM:** An introduction to Operating Systems-ARM System Control coprocessor-CP15 Protection unit registers-ARM protection unit-CP15 MMU registers-ARM Architecture-Synchronization-Context Switching input and outputDetection of discontinuities, Edge linking and boundary detection, Thresholding,	CO-5	1.What is coprocessor, how it is useful for SOC. 2. Write a short note on context switching and edge linking.	▫ Lecture ▫ Discussion	Mid-Test 2 (Week 14-18)

	Region oriented segmentation.				
18	**Mid-Test 2**	CO-1 & CO-2			(Week 19)
19/20	**END EXAM**				