SCHEME OF COURSE WORK

Course Details:

Course Title	: **LOW POWER VLSI DESIGN**		
Course Code	**:** 13EC2211	**L T P C**	**:4 0 0 3**
Program:	**: M. Tech**		
Specialization:	**: VLSI Design and Embedded Systems**		
Semester	**: I**		
Prerequisites	**:VLSI TECHNOLOGY AND DESIGN**		
Courses to which it is a prerequisite	**: ANALOG IC DESIGN**		

Course Outcomes (COs):

1	Illustrate the design limitations of Low Power VLSI Design and Evolution of SOI Technologies.
2	Describe various integration and isolation techniques for MOS/Bi-CMOS Technologies.
3	Obtain proficiency in parameter extraction of Bi-polar, MOSFETS using SPICE and Advanced MOSFET models.
4	Design and analyze Conventional CMOS and Bi-CMOS logic gates.
5	Design low voltage, low power Bi-CMOS logic circuits to achieve High Performance.

Course Outcome Vs **Program Outcomes:**

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO-1	S	S	S	S	S	S			M		M
CO-2	S	S	S	S	S	S			M		M
CO-3	S	S	S	S	S	S			M		M
CO-4	S	S	S	S	S	S			M		M
CO-5	S	S	S	S	S	S			M		M

S - Strongly correlated, *M - Moderately* correlated, *Blank - No correlation*

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Teaching-Learning and Evaluation

Week	TOPIC / CONTENTS	Course Outcomes	Sample questions	TEACHING-LEARNING STRATEGY	Assessment Method & Schedule
1	**UNIT-I** Introduction, Overview & Importance of Low Power VLSI Designs, Low Power Design Limitations: Power supply voltage, Threshold voltage, Scaling, Interconnect wires.	CO-1	1.Explain the advantages of low power requirement in VLSI? 2. Discuss the limitations of low power design? 3. Explain how Bi-	▫ Lecture ▫ Discussion	Mid-I/Assignment - I

			CMOS technology is useful for low power VLSI?		
2	Silicon-on-Insulator (SOI) From Devices to Circuits. **UNIT-II** Realization of Bi-CMOS processes, Bi-CMOS manufacturing and Integration Considerations: Hot carrier Effect and methods to overcome it.	CO-2	1.Explain with neat structures the construction of : i) SBC Bi-CMOS structure. ii) Twin-well Bi-CMOS structure?	▫ Lecture ▫ Discussion	Mid-I/Assignment -I
3	Production of Graded-drain structures, Phosphorus drain structures, Double diffused drain structures, Lightly doped drain structures.	CO-2	Discuss the process considerations for BJTs in the fabrication of Bi-CMOS devices?	▫ Lecture ▫ Discussion	Mid-1/Assignment -1
4	Isolation in Bi-CMOS: Deep trench techniques, LOCOS Structures, Advanced Isolation techniques.	CO-2	Explain junction isolation and LOCOS isolation techniques?	▫ Lecture ▫ Discussion	Mid-I/Assignment -I
5	Typical modern processing steps and high performance Bi-CMOS structures, Future trends and directions of CMOS/Bi-CMOS processes.	CO-3	What are the future trends and directions of CMOS/Bi- CMOS processes?	▫ Lecture ▫ Discussion ▫ Power point lectures	Mid-I/Assignment -I
6	**UNIT-III** The MOS (FET) Transistor, The Bipolar (Junction) transistor, Device Fabrication	CO-3	Discuss the salient features of level-1 and level-2 models for simulating the performance of MOSFETs?	▫ Lecture ▫ Discussion ▫ Power point lectures	Mid-I/Assignment -I
7	MOSFET Simulation models: Level 1,2,3,14, Advanced BSIM Models, Eber-Moll model, H- Spice level-50 model, EKV MOSFET Model.	CO-3	Explain the Ebers-Moll model for BJTs with equivalent circuits.	▫ Lecture ▫ Discussion ▫ Programming	MidII/ /Assignment II/SEMINAR
8	Bipolar Spice models: Gummel-poon model, and its modified model.	CO-3	Explain the Gummel-poon model for BJTs with equivalent circuits.	▫ Lecture ▫ Discussion ▫ Power point lectures	MidII/ /Assignment II/SEMINAR
9	**Mid-Test 1**	CO-1, CO-2 &CO-3			

10	Sub-half micron devices, MOSFET in Hybrid mode Environment – Surface p – channel for Sub-half-Micron Devices.	CO-3	Discuss the characteristics of MOSFET in Hybrid mode Environment?	▫ Lecture ▫ Discussion ▫ Power point lectures	MidII/ /Assignment II/SEMINAR
11	Device Fabrication, Model parameters Extraction, Sub-Half-Micron D.C. Model Formulation.	CO-3	Explain analytical and experimental characterization of sub-half micron MOS devices?	▫ Lecture ▫ Discussion ▫ Power point lectures	MidII/ /Assignment II/SEMINAR
12	**UNIT-IV** Conventional CMOS Logic gates, Conventional Bi-CMOS Logic gates, their power dissipation and characteristics	CO-4	Explain the working of a basic conventional Bi-CMOS inverter?	▫ Lecture ▫ Discussion ▫ Power point lectures	MidII/ /Assignment II/SEMINAR
13	Bi-CMOS Circuits Utilizing Lateral PnP BJTs in PMOS structures, Performance Evaluation and Comparison.	CO-4	Illustrate the construction of lateral PnP BJT in PMOS Structure and explain the current components in such a device in its hybrid-mode environment?	▫ Lecture ▫ Discussion ▫ Power point lectures	Mid II/ /Assignment II/SEMINAR
14	**UNIT-V** Merged Bi-CMOS digital circuits, Full-Swing Multidrain/ Multicollector Complementary Bi-CMOS Buffers.	CO-5	Explain about Merged Bi-CMOS digital circuits?	▫ Lecture ▫ Discussion ▫ Power point lectures	MidII/ /Assignment II/SEMINAR
15	Quasi-complementary Bi-CMOS Digital circuits, Full-Swing Bi-CMOS /Bi-NMOS Digital circuits employing Schottky Diodes, Feedback type Bi-CMOS digital circuits.	CO-5	Discuss the basic driver circuits and their modifications to obtain the full swing complementary MOS Bipolar logic (FS-CMBL) circuits?	▫ Lecture ▫ Discussion	MidII/ /Assignment II/SEMINAR
16	High-Beta Bi-CMOS digital circuits, Transiently saturated Full-Swing Bi-CMOS Digital circuits, ESD-free Bi-CMOS Digital circuit- circuit operation and comparative Evaluation.	CO-5	Explain the principle of ESD-Free Bi-CMOS circuit?	▫ Lecture ▫ Discussion	MidII/ /Assignment II/SEMINAR
17	Evolution of Latches and Flip-Flops, Quality measures for Latches and Flip-Flops and Design Perspective.	CO-5	What are different quality measures for Latches and Flip-Flops?	▫ Lecture ▫ Discussion	MidII/ /Assignment II/SEMINAR
18	**Mid-Test 2**	CO-3,			

		CO-4& CO-5			
19/20	**END EXAM**				