SCHEME OF COURSE WORK

Course Details:

Course Title	: EMBEDDED COMPUTING SYSTEMS		
Course Code	**:** 13EC2206	**L T P C**	**:4 0 0 3**
Program:	**: M.Tech**		
Specialization:	**: VLSI Design and Embedded Systems**		
Semester	**: I**		
Prerequisites	**: System On Chip Architecture**		
Courses to which it is a prerequisite	**: Embedded systems**		

Course Outcomes (COs):

CO1	Comprehend concepts of UML architectures, CPU architectures BUS architectures for Embedded computations.
CO2	Design of generic compilers for Embedded systems and its test procedures.
CO3	Demonstrate operating system concepts
CO4	Discuss real time task scheduling context switching.
CO5	Outline design aspects of real-time operating system, modeling and working on Real-time environment.

Course Outcome Vs **Program Outcomes:**

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO-1	S	S	S	S	S							S
CO-2	S	S	S	S	S							M
CO-3	S	S	S	S	S							S
CO-4	S	S	S	S	S	M						S
CO-5	S	S	S	S	S	S	M					S

S - Strongly correlated, *M - Moderately* correlated, *Blank - No correlation*

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Teaching-Learning and Evaluation

Week	TOPIC / CONTENTS	Course Outcomes	Sample questions	TEACHING-LEARNING STRATEGY	Assessment Method & Schedule
1	**UNIT-I** **INTODUCTION:** **INTRODUCTION TO DESIGN AND ARCHITECTURE:** Requirements, specifications, structural and behavioral descriptions, UML; Embedded Processors: RISC, super scalar, and VLIW architectures, memory organization	CO-1	1.Describe different structural components of UML diagram. 2. Differentiate between CISC and RISC processors.	▫ Lecture ▫ Discussion	(Week 1- 3)

	and Instruction level parallelism; CPU architectures: Input/output, interrupts, modes, cache memories Embedded bus architectures: Bus architectures and transactions, Serial interconnects, Networked embedded systems: Bus protocols, I2C bus and CAN bus; Internet-Enabled Systems, Design Example-Elevator Controller				
2	**UNIT-II** **DESIGN OF COMPILERS:** Compilers and optimization. Testing, Performance Analysis, Hardware Accelerators: FPGA architectures, RISC IP Cores, Verilog HDL.	CO-2	1. Discuss different design aspects of compilers for sensors. 2. Explain FPGA networks and its advantages.	▫ Lecture ▫ Discussion	(Week 4-6)
3	**UNIT-III** **OPERATING SYSTEMS &RTOS-I:** Operating system concepts: Embedded operating systems ,Network operating systems, Layers, functions kernel, Tasks, Scheduling Thread, Interrupt process, communication, Device drivers, codes, pseudo codes for OS.Introduction, Modeling Timing constraints Scheduling Real-Time Tasks: Types of Schedulers Table-driven scheduling cyclic schedulers EDF RMA.	CO-3	1. Explain the concept of scheduling algorithms. 2. What is the purpose of device drivers and explain design of drivers for USB Port	▫ Lecture ▫ Discussion ▫ NPTEL	Assignment 1 (Week 7- 8)
4	**MID-TEST 1**			▫	(Week 9)
5	**UNIT-IV** **OPERATING SYSTEMS & RTOS-II:** Handling Resource sharing among real-time tasks Scheduling Real-Time Tasks in Multiprocessor and Distributed systems Commercial Real-time operating systems: Tasks, context switches, Operating system support (inter-process communication, networking), Scheduling, Development environment.	CO-4	1. Name few RTOS Systems 2.Distinguish between hard, firm and sporadic real time tasks.	▫ Lecture ▫ Discussion ▫ NPTEL	(Week 10 - 13)

6	**UNIT-V** **DESIGN COMPUTATIONS &EMBEDDED SYSTEM APPLICATION:** Database Systems, Product design process and testing Design Computations Design challenge – optimizing design metrics, processor technology, design technology; real time-operating system: system modeling, static scheduling, Priority drive scheduling, Synchronization & mutual exclusion (real-time and non-real-time); H/W and S/W co-design; embedded multiprocessor.	CO-5	1. Discuss design challenges for optimizing design in RTOS. 2. Differentiate between hardware and software code design.	▫ Lecture ▫ Discussion	Assignment 2 (Week 14-18)
7	**Mid-Test 2**	CO-1 & CO-2			(Week 19)
19/20	**END EXAM**				