SCHEME OF COURSE WORK

Course Title	:Electronic Design Automation Tools		
Course Code	:13EC2213	L T P C	4 0 0 3
Program:	:M.Tech		
Specialization:	: Embedded Systems and VLSI Design		
Semester	:II		
Prerequisites	: Digital IC Applications, Electronic Circuits ,Digital Design Through Verilog, VLSI Design		
Courses to which it is a prerequisite	: To carry out further Research Work in VLSI design		

Course Outcomes (Cos):

1	Illustrate different simulations and delay models which are available for HDL.
2	Classify the different synthesis using CAD tools.
3	Design And Analyze Analog And Digital Circuits Using PSPICE model of Transistor.
4	Describe about Analog, Digital & Mixed Signal Simulators.
5	Illustrate PCB Design and also describe the tools used for PCB design.

Course Outcomes versus Program Outcomes:

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	**S**	**S**	**S**	**S**	**S**				**S**		**S**
CO2	**S**	**S**	**S**	**S**	**S**				**S**		**S**
CO3	**S**	**S**	**S**	**S**	**S**				**S**		**S**
CO4	**S**	**S**	**M**	**S**	**S**				**S**		**S**
CO5	**S**	**S**		**S**	**S**	**S**			**S**		**S**

S - Strongly correlated, M - Moderately correlated, Blank - No correlation

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Week	Topic /Contents	Course Outcomes	Sample questions	Teaching-Learning Strategy	Assessment Method & Schedule
1	Simulation-Types of Simulation, Logic Systems, Working of Logic Simulation	CO1	1. Describe about conditional, procedural, continuous and non-blocking assignments with their syntaxes and examples. 2. Define the terms 'Simulation' and 'Synthesis' relevant to HDLs. Explain them with suitable block diagrams.	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
2	Cell Models, Delay Models, State Timing Analysis	CO1	1. What are the two kinds of delays that can be specified in a procedural assignment statement? Elaborate using an example. 2. What is static timing Analysis? Explain briefly with suitable example	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
3	Formal Verification, Switch-Level Simulation, Transistor-Level Simulation	CO1	1.Explain in detail the following i) Switch-level ii) Transistor-level simulations. 2. Explain about various simulations and their significance with neat flow diagram.	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
4	Verilog and Logic Synthesis, VHDL and Logic Synthesis	CO2	1.Model an USR and write a verilog code for it and analyse synthesized net list for this model. 2. Write verilog code for 4 to 1 multiplexer using procedural continuous assignments.	Lecture/ Discussion/ Programming	Assignment I/Quiz-I/Mid-I

5	Memory Synthesis, FSM Synthesis, Memory Synthesis, Performance-Driven Synthesis.	CO2	1.Explain about FSM synthesis and performance driven synthesis 2. Model a synthesizable RAM memory using VHDL.	Lecture/ Discussion/ Programming	Assignment I/Quiz-I/Mid-I
6	CAD Tools for Simulation and Synthesis: Modelsim and Leonardo Spectrum	CO2	1. Write the features of MODELSIM. 2. Explain Synthesis Procedure in Leonardo Spectrum.	Lecture/ Discussion/ Programming	Assignment I/Quiz-I/Mid-I
7	Pspice Models For Transistors	CO3	1.Explain about PSPICE Models for transistors. 2. Draw the two stage BJT amplifier in self bias mode coupled by R_C network with R_S = 150Ω, coupling capacitors $C_1 = C_2$ = 10 μ F, R_1 and R_2 in the first stage, R_1 = 200kΩ, R_2 = 50kΩ, R_{c1} = 12Ω, R_{e1} = 3.6kΩ, C_{e1} = 15 μ F. In second stage: R_1 = 120KΩ, R_2 = 30kΩ, R_{c2} = 6.8kΩ , C_{e2} = 25 μ F with Rc = 10kΩ and V_{CC} = 15V. Draw its Pspice schematic and using of the Pspice circuit file. Draw its frequency response circuit with Vin = 1mv (P-to-P).	Lecture/ Discussion/ Programming	Assignment I/Quiz-I/Mid-I
8	A/D & D/A Sample And Hold Circuits etc., and Digital System Building Blocks	CO3	1.Explain about the design considerations and simulation procedure for D/A converter circuit using PSPICE Software tool 2. Explain PSPICE model for S/H circuit	Lecture/ Discussion/ Programming	Assignment I/Quiz-I/Mid-I
9	Mid-Test-1	--		------	----------

10	Design and Analysis of Analog Circuits Using PSPICE.	CO3	1.Write spice code for op-amp based integrator to get transient response. 2. Design a two stage RC coupled amplifier and analyze it using PSPICE. Assume the data needed.	Lecture/ Discussion/ Programming	Assignment II/Quiz-II/Mid-II
11	Design and Analysis of Digital Circuits Using PSPICE.	CO3	1.Write spice code for Half Adder circuit. 2. Design a D Flip-Flop using PSpice. Assume the data needed.	Lecture/ Discussion/ Programming	Assignment II/Quiz-II/Mid-II
12	Fundamentals Of Analog And Digital Simulation,	CO4	1. Explain the fundamentals of Analog, Digital and Mixed signal simulators in VLSI design. 2. Explain about Event driven simulation with an example.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
13	Mixed Signal Simulator Configurations	CO4	1.Explain the analysis of A/D converter in mixed signal VLSI Design 2. List out and explain different approaches for modeling the mixed signal circuits.	Lecture/ Discussion/ Programming	Assignment II/Quiz-II/Mid-II
14	Understanding Modeling, Integration To CAD Environments.	CO5	1.Name different CAD tools for simulation and synthesis and explain them in detail 2. Explain the analysis of up converter using the relevant CAD environment.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
15	An Overview of High Speed PCB Design	CO5	1.Explain various issues involved in high speed PCB design. 2.Explain about High	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II

			Speed PCB Layout techniques.		
16	Design Entry, Simulation and Layout Tools for PCB,	CO5	1.Explain the simulation and layout tools for PCB Design 2.What are the various software tools available for PCB design and layout? Briefly discuss about them.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
17	Introduction to Orcad PCB Design Tools.	CO5	1. Explain in detail ORCAD PCB design tools 2. Explain about 'ORCAD component information' system with the help of neat block diagram.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
18	Mid-Test 2	------	----------		
19/20	END EXAM	------	------		