SCHEME OF COURSE WORK

Course Details:

Course Title	: **DSP PROCESSORS & ARCHITECTURE**		
Course Code	**: 13EC1138**	**L T P C**	**:4 0 0 3**
Program:	**: B.Tech**		
Specialization:	**: Electronics & Communication Engineering**		
Semester	**: VIII**		
Prerequisites	**: Signals And Systems, Digital Signal Processing**		
Courses to which it is a prerequisite	**: --**		

Course Outcomes (COs):

CO1	Comprehends the concepts of digital signal processing techniques.
CO2	Design DSP computational building blocks to achieve high speed in DSP processor.
CO3	Comprehends DSP TMS320C54XX architecture and instructions.
CO4	Develop DSP algorithms using DSP processor.
CO5	Interface memory, I/O peripherals and Serial communication devices to DSP processors.

Course Outcome Vs **Program Outcomes:**

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO-1	S	S	S	S	S	M			M			M
CO-2	S	S	S	S	S	M			M			M
CO-3	S	S	S	S	S	M			S			M
CO-4	S	S	S	S	S	M			M			M
CO-5	S	S	S	S	S	M			S			S

S - Strongly correlated, *M - Moderately* correlated, *Blank - No correlation*

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Teaching-Learning and Evaluation

Week	**TOPIC / CONTENTS**	**Course Outcome**	**Sample questions**	**TEACHING-LEARNING STRATEGY**	**Assessment Method & Schedule**
1	**UNIT-I** Introduction, A Digital signal processing system, The sampling process, discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier transform (FFT).	CO-1	1.a) Define a DFT pair. b) Explain the phenomenon of Aliasing? 2. Explain about Convolution, Decimation and Interpolation?	▫ Lecture ▫ Discussion ▫ Programming	Mid-1/Quiz-1/ Assignment 1

2	linear time- invariant systems, Digital filters, Decimation and interpolation, Number formats for signals and coefficients in DSP systems,	CO-1	1. Draw the block diagram of Digital filter structure? 2. If decimation by a factor of 8 is achieved by decimating by a factor of 2 followed by another factor of 4, Determine the cut off frequencies of the two low pass filters that should be used in the decimation?	▫ Lecture ▫ Discussion ▫ Programming	Mid-1/Quiz-1/ Assignment -1
3	Dynamic range and Precision, Sources of error in DSP implementations, A/D conversion error, DSP computational errors, D/A conversion errors.	CO-1	1.Specify basic architecture required to implement following operation so that they can be executed in least possible time i) (x1+jy1)*(x2+jy2) ii) 0.5 (x1+4x2)/256	▫ Lecture ▫ Discussion	Mid-1/Quiz-1/ Assignment -1
4	**UNIT-II** Basic architectural features, DSP computational building blocks, bus architecture and memory.	CO-2	1.Explain how a DSP processor got specialized features in terms of its architectures?	▫ Lecture ▫ Discussion	Mid-1/Quiz-1/ Assignment -1
5	Data addressing capabilities, address generation unit, programmability and program execution, Speed issues, Hardware looping.	CO-2	1.Write a short note on speed issues of DSP processors?	▫ Lecture ▫ Discussion	Mid-1/Quiz-1/ Assignment -1
6	Interrupts, Stacks, Relative branch support, Pipelining and performance.	CO-2	1) How can achieve system level parallelism & pipelining for 8 coefficients FIR filter? 2) Implement the 8 coefficient FIR filter design using single and two MAC units?	▫ Lecture ▫ Discussion	Mid-1/Quiz-1/ Assignment 1
7	Pipelined Depth, Interlocking, branching effects, pipeline programming models.	CO-2		▫ Lecture ▫ Discussion	Mid-1/Quiz-1/ Assignment 1
8	**UNIT-III** Commercial digital signal processing devices, Data addressing modes of TMS320C54XX DSPs, data addressing modes of TMS320C54XX processors.	CO-3	1.Explain the functional diagram of CPU TMS320C54XX processor? 2. Explain the multiplier/adder functional diagram of	▫ Lecture ▫ Discussion	Mid-1/Quiz-1/ Assignment 1

			CPU TMS320C54XX processor?		
9	**Mid-Test 1**	CO-1,2 &CO-3			MID TEST-I
10	Memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, On-Chip peripherals.	CO-3	1.Explain about TMS320C54XX processor buses, internal memory organization and CPU?	▫ Lecture ▫ Discussion ▫ Programming	MID-2/QUIZ-II/ Assignment 2
11	Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX processors. **UNIT-IV** The Q-notation, FIR filters.	CO-3	1.Write a short note on Interrupt Mask Register(IMR)/ Interrupt flag register(IFR)?	▫ Lecture ▫ Discussion ▫ Programming	MID-2/QUIZ-II/ Assignment 2
12	IIR filters, interpolation filters, Decimation filters, PID controller, adaptive filters, An FFT algorithm for DFT computation.	CO-4	1. Write a code to implement direct form of adaptive FIR filter using least mean square algorithm?	▫ Lecture ▫ Discussion ▫ Programming	MID-2/QUIZ-II/ Assignment 2
13	A Butterfly computation, Overflow and scaling, Bit-reversed index generation, An 8-pointr FFT implementation on the TMS320C54XX.	CO-4	1.Write a code for implementation of 9-tap adaptive filter for TMS320C54XX processor?	▫ Lecture ▫ Discussion ▫ Programming	MID-2/QUIZ-II/ Assignment 2
14	Computation of the signal spectrum. **UNIT-V** Memory space organization, External bus interfacing signals.	CO-4	1.Explain how memory and parallel I/O peripherals are interfaced using external bus?	▫ Lecture ▫ Discussion	MID-2/QUIZ-II/ Assignment 2
15	Memory interface, Parallel I/O interface, programmed I/O, interrupts and I/O.	CO-5	Explain how to interface parallel I/O peripherals to programmable DSP devices with an example?	▫ Lecture ▫ Discussion	MID-2/QUIZ-II/ Assignment 2
16	Direct memory access (DMA), A Multichannel buffered serial port(McBSP).	CO-5	Explain the operation of multichannel buffer serial port McBSP with block diagram?	▫ Lecture ▫ Discussion	MID-2/QUIZ-II/ Assignment 2
17	McBSP programming, a CODEC interface circuit, CODEC programming, A	CO-5	1.Mention the program registers of PCM 3002 CODEC?	▫ Lecture ▫ Discussion ▫ Programming	MID-2/QUIZ-II/ Assignment 2

	CODEC-DSP interface example.		2.Explain how to configure the CODEC using mode control interface signals?		
18	**Mid-Test 2**	CO-3,4& CO-5			MID TEST-II
19/20	**END EXAM**				