SCHEME OF COURSE WORK

Course Details:

Course Title	: **DIGITAL DESIGN THROUGH HDL**							
Course Code	**: 13EC2203**	**L**	**T**	**P**	**C**	**:4**	**0**	**0**	**3**
Program:	**: M.Tech.**							
Specialization:	**: VLSI Design and Embedded Systems**							
Semester	**: I**							
Prerequisites	**:STLD**							
Courses to which it is a prerequisite	**: --**							

Course Outcomes (COs):

1	Distinguish dataflow, behavioral and structural design elements inVHDL.
2	Outline the basic concepts of Verilog language.
3	Classify gate level modeling and dataflow level modeling.
4	Distinguish behavioral level modeling and switch level modeling.
5	Design Finite state machines and comprehend concepts of functions, tasks, and user defined primitives.

Course Outcome Versus **Program Outcomes:**

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**
CO-1	S	S		S	S				M		
CO-2	S	S		S	S				M		
CO-3	S	S		S	S				M		
CO-4	S	S		S	S				M		
CO-5	S	S		S	S				M		

S - Strongly correlated, *M* - *Moderately* correlated, *Blank* - *No correlation*

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Teaching-Learning and Evaluation

Week	**TOPIC / CONTENTS**	**Course Outcomes**	**Sample questions**	**TEACHING-LEARNING STRATEGY**	**Assessment Method & Schedule**
1	**Combinational and Sequential Logic Design Using VHDL:** Data flow design elements, behavioral design elements, Structural design elements, simulation and synthesis	CO-1	1.Design the logic circuit and write a data-flow style VHDL program for the following function? $F(X) = \sum A,B,C,D\ (3, 5, 6, 7, 10, 13, 14) + d\ (1, 2, 4, 15)$ 2. Explain the three modeling styles in VHDL with an example.	▫ Lecture ▫ Discussion ▫ Programming	Mid1/Assignment 1
2	**Combinational and Sequential Logic Design Using VHDL:** decoders, multiplexers, comparators, ALUs	CO-1	1. Design a 32 to 1 multiplexer using four 74×151 multiplexers and 74X139	▫ Lecture ▫ Discussion ▫ Programming	Mid1/Assignment 1

			decoder. Write a VHDL program for the same in structural modeling style. 2. Design an 8-bit comparator using 74x85 ICs		
3	**Combinational and Sequential Logic Design Using VHDL:** Latches and flip-flops, counters, shift registers.	CO-1	1. Write a VHDL program for a 4-bit serial in parallel out right shift register .	▫ Lecture ▫ Discussion ▫ Programming	Mid1/Assignment 1
4	**Introduction to Verilog:** Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools	CO-2	1.Briefly describe the basic modeling styles supported by Verilog HDL . 2. Define and explain the following terms relevant to Verilog HDL. 1. Module 2. Test bench	▫ Lecture ▫ Discussion ▫ Programming	Mid1/Assignment 1
5	**Introduction to Verilog:** Test Benches. Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators.	CO-2	1.Explain about following Language constructs and conventions in Verilog. 1.Identifiers 2.Numbers 3.Strengths 4.Data types 5.Comments 2.What are the various data types available in Verilog HDL. Explain them with necessary syntax and suitable example.	▫ Lecture ▫ Discussion ▫ Programming	Mid1/Assignment 1
6	**Introduction to Verilog:** System Tasks, Functions, and Compiler Directives: Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations.	CO-2	1. Explain about System Tasks in Verilog HDL 2. Write about standard compiler directives used in Verilog HDL	▫ Lecture ▫ Discussion ▫ Programming	Mid1/Assignment 1
7	**GATE LEVEL MODELING:** Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples	CO-3	1. Implement the gate level description of a 2 to 4 decoder circuit with relevant logic diagram and Verilog HDL source code. 2. Implement gate level description of a 4 to 1 multiplexer circuit with relevant logic diagram and Verilog HDL source code.	▫ Lecture ▫ Discussion ▫ Programming	Mid1/Assignment 1
8	**GATE LEVEL MODELING:** Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip-flops with Gate Primitives	CO-3	1. Implement the gate level description of a JK Flip flop	▫ Lecture ▫ Discussion ▫ Programming	Mid1/Assignment 1
9	**Mid-Test 1**	CO-1 , CO2,CO-3	----------	---------	----

10	**GATE LEVEL MODELING:** Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits. **DATA FLOW LEVEL MODELING:** Introduction, Continuous Assignment Structures	CO-3	1. Describe the following relevant to gate level modeling with necessary syntax and example.1. Gate delays 2. Strengths and contention Resolution	▫ Lecture ▫ Discussion ▫ Programming	Mid2 /Assignment 2
11	**DATA FLOW LEVEL MODELING:** Delays and Continuous Assignments, Assignment to Vectors, Operators.	CO-3	1. Describe the continuous assignment feature of Verilog HDL with suitable example. 2. Write a Dataflow level description for a BCD adder	▫ Lecture ▫ Discussion ▫ Programming	Mid2 /Assignment 2
12	**BEHAVIORAL MODELING:** Introduction, Operations and Assignments, Functional Bifurcation, *Initial* Construct, *Always* Construct, Examples	CO-4	1. Implement the behavioral level description of a JK Flip flop circuit using an always statement and draw the synthesized circuit.	▫ Lecture ▫ Discussion ▫ Programming	Mid2 /Assignment 2
13	**BEHAVIORAL MODELING:** Assignments with Delays, *Wait* construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-blocking Assignments, The case statement, Simulation Flow. I*f* and i*f*-else constructs	CO-4	1.Write a behavioral level description of 4-bit up/down counter. 2. Write a Verilog HDL source code for clocked RS flip flop and draw the relevant synthesized circuit along with simulation results.	▫ Lecture ▫ Discussion ▫ Programming	Mid2 /Assignment 2
14	**BEHAVIORAL MODELING:** assign-deassign construct, repeat construct, for loop, the disable construct, whileloop, forever loop, parallel blocks, force-release construct, Event.	CO-4	1. Explain different Loop statements with necessary syntax and relevant example. 2. Write about the following statements with exam (i)If statement (ii)Case statement (iii)Loop statement	▫ Lecture ▫ Discussion ▫ Programming	Mid2 /Assignment 2
15	**SWITCH LEVEL MODELING:** Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets.	CO-4	1. What are the various switch level primitives and give their instantiations .Draw the basic CMOS inverter circuit and write its Verilog HDL source code. 2. Write a switch level description for a 2 input NMOS NOR gate with active pull up load.	▫ Lecture ▫ Discussion ▫ Programming	Mid2 /Assignment 2
16	**Functions, Tasks and User-Defined Primitives:** Introduction, Function, recursive functions, Tasks, User-Defined Primitives (UDP)-combinational UDPs, sequential UDPs	CO-5	1.Define User defined primitives with syntax. Explain the difference between combinational and sequential UDP s with examples.	▫ Lecture ▫ Discussion ▫ Programming	Mid2 /Assignment 2
17	**FSM DESIGN:** Moore and Mealy Machines.	CO-5	1. Draw the state diagram and state Machine chart for the synchronous circuit having following description:(i) The circuit has control input C,clock and outputs a,b,c.(ii)If C=1,on	▫ Lecture ▫ Discussion ▫ Programming	Mid2 /Assignment 2

			every positive edge of the clock the output changes in the sequence:000→001→011→111→000 and repeats.(iii)If C=0,the circuit holds in the present state i.e in the same state		
18	**Mid-Test 2**	CO-3,CO-4,CO5	**----------**	**----------**	------
19/20	**END EXAM**				