SCHEME OF COURSE WORK

Course Title	: Digital IC Design		
Course Code	: 13EC1125	L T P C	4 0 0 3
Program:	: B.Tech		
Specialization:	: Electronics and Communication Engineering		
Semester	: VI		
Prerequisites	: VLSI Design, Switching Theory & Logic Design		
Courses to which it is a prerequisite	:		

Course Outcomes (Cos):

1	Analyze the depth of designing a Digital IC and use the concept of logical effort for Transistor sizing.
2	Obtain Proficiency in SPICE modeling of CMOS circuits.
3	Describe the various design entities.
4	Distinguish between Static CMOS design and Dynamic CMOS design.
5	Design Logic gates, Flip-flops, Adders, Registers and RAM etc.

Course Outcomes versus Program Outcomes:

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**S**	**S**										**M**
CO2	**S**	**M**			**M**							**M**
CO3	**S**	**M**	**M**									**M**
CO4	**S**	**S**	**M**	**M**								**M**
CO5	**S**	**S**	**M**	**M**								**M**

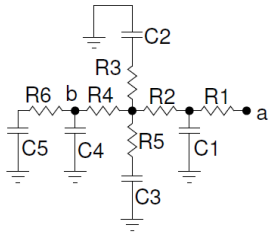
S - Strongly correlated, M - Moderately correlated, Blank - No correlation

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

<table>
<tr><th>Week</th><th>Topic /Contents</th><th>Course Outcomes</th><th>Sample questions</th><th>Teaching-Learning Strategy</th><th>Assessment Method & Schedule</th></tr>
<tr><td>1</td><td>Historical Perspective, Issues in Digital Integrated Circuit Design,
Quality Metrics of a Digital Design: Cost of an Integrated Circuit, Functionality and Robustness, Performance, Power and Energy Consumption.</td><td>CO1</td><td>1. Explain the quality metrics of a digital IC design.

2. Define Moore’s law. Explain the historical perspective and issues in digital IC design.</td><td>Lecture/ Discussion</td><td>Assignment-I/Quiz-I/Mid-I</td></tr>
<tr><td>2</td><td>The MOS Transistor under Static Conditions.</td><td>CO2</td><td>1. The data from five measurements made on a short channel NMOS device appears in below Table. Given that V_{DSAT}= 0.6 V and k’ = 100 μA/V^2, calculate V_{T0},γ, λ, 2| φ_F|, and W/L.
<table>
<tr><th>No.</th><th>V_{GS}</th><th>V_{DS}</th><th>V_{BS}</th><th>I_D(μA)</th></tr>
<tr><td>1</td><td>2.5</td><td>1.8</td><td>0</td><td>1812</td></tr>
<tr><td>2</td><td>2</td><td>1.8</td><td>0</td><td>1297</td></tr>
<tr><td>3</td><td>2</td><td>2.5</td><td>0</td><td>1361</td></tr>
<tr><td>4</td><td>2</td><td>1.8</td><td>-1</td><td>1146</td></tr>
<tr><td>5</td><td>2</td><td>1.8</td><td>-2</td><td>1039</td></tr>
</table>
2. Explain the effect of velocity saturation on short channel devices and compare it with long channel devices.</td><td>Lecture/ Problem solving</td><td>Assignment-I/Quiz-I/Mid-I</td></tr>
<tr><td>3</td><td>Dynamic Behavior, The Actual MOS Transistor-Some Secondary Effects</td><td>CO2</td><td>1. Determine the high-to-low propagation delay for an inverter with a 500nm wide NMOSFET and a 1 μm wide PMOSFET with its output connected to another identical inverter. Assume the default 250nm process. Do consider overlap capacitance. Recall that it is necessary to consider both bottom and sidewall capacitance. You may neglect the resistance and capacitance of the wire connecting the two inverters.

2. Explain the threshold variation and Hot-Carrier effects of a MOS transistor.</td><td>Lecture/ Problem solving</td><td>Assignment-I/Quiz-I/Mid-I</td></tr>
<tr><td>4</td><td>SPICE Models for the MOS Transistor, Method of Logical Effort for transistor sizing.</td><td>CO2</td><td>1. Explain the methods of logical effort for transistor sizing with necessary examples.</td><td>Lecture/ Discussion</td><td>Assignment-I/Quiz-I/Mid-I</td></tr>
</table>

5	WIRE: Introduction, A First Glance, Interconnect Parameters - Capacitance, Resistance, and Inductance, Electrical wire models, SPICE wire models.	CO2	1. Explain the following interconnect parameters a) Capacitive b) Inductive c) Resistance 2. Determine the Elmore delay from Node a to Node b in the following circuit.  	Lecture/ Problem solving	Assignment-I/Quiz-I/Mid-I
6	Introduction, The Static CMOS Inverter-An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Switching Threshold, Noise Margins, Robustness Revisited	CO3	1. Give an intuitive perspective of the static CMOS inverter with relevant diagrams. 2. Deduce the noise margins of the CMOS inverter.	Lecture/ Problem solving	Assignment-I/Quiz-I/Mid-I
7	Performance of CMOS Inverter: The Dynamic Behavior, Computing the Capacitances.	CO3	1. Explain the dynamic behavior of CMOS inverter. 2. Represent the parasitic capacitances of a CMOS inverter.	Lecture/ Problem solving	Assignment-I/Quiz-I/Mid-I
8	Propagation Delay: First-Order Analysis, Propagation Delay from a Design Perspective.	CO3	1. Deduce propagation delay of CMOS inverter. 2. Explain design techniques to minimize propagation delay of a gate.	Lecture/ Discussion	Assignment-I/Quiz-I/Mid-I
9	Mid-Test-1	--	---------	------	----------
10	Power, Energy, and Energy-Delay: Dynamic Power Consumption, Static Consumption, Perspective: Technology Scaling and its Impact on the Inverter Metrics.	CO3	1. List the different types of power consumption of a CMOS inverter? 2. Explain the technology Scaling effects and its impact on the inverter metrics.	Lecture/ Problem solving	Assignment-II/Quiz-II/Mid-II
11	DESIGNING COMBINATIONAL LOGIC GATES IN CMOS: Introduction, Static CMOS Design: Complementary CMOS, Ratioed Logic, Pass-Transistor Logic.	CO4	1. Given the choice between NOR and NAND logic. Which one would you prefer for implementation in complementary CMOS and pseudo-NMOS? State why? 2. Explain how to overcome transistor-sizing problem in level restoring circuits.	Lecture/ Discussion	Assignment-II/Quiz-II/Mid-II
12	Dynamic CMOS Design: Dynamic Logic - Basic Principles, Speed and Power Dissipation of Dynamic	CO4	1. What are the signal integrity issues in Dynamic CMOS design? How to overcome those?	Lecture/ Discussion	Assignment-II/Quiz-II/Mid-II

	Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Perspectives: How to Choose a Logic Style, Designing Logic for Reduced Supply Voltages		2. Explain the optimization of domino logic gates.		
13	DESIGNING SEQUENTIAL LOGIC CIRCUITS: Introduction, Timing Metrics for Sequential Circuits, Classification of Memory Elements, Static Latches and Registers: The Bi-stability Principle	CO5	1. Explain the timing metrics for sequential circuits. 2. Explain the bi-stability principle with the help of appropriate diagrams.	Lecture/ Discussion	Assignment-II/Quiz-II/Mid-II
14	Multiplexer-Based Latches, Master-Slave Edge-Triggered Register, Low-Voltage Static Latches, Static SR Flip-Flops—Writing Data by Pure Force	CO5	1. Explain the operation of negative and positive latches based on multiplexers. 2. Explain the operation of master slave positive edge triggered register using multiplexers. Also narrate the corresponding timing properties.	Lecture/ Discussion	Assignment-II/Quiz-II/Mid-II
15	Dynamic Latches and Registers: Dynamic Transmission-Gate Edge-triggered Registers, C^2MOS—A Clock Skew Insensitive Approach, True Single-Phase Clocked Register (TSPCR)	CO5	1. Explain the operation of C^2MOS based dual edge triggered register. 2. Design –ve edge triggered register in TSPC.	Lecture/ Discussion	Assignment-II/Quiz-II/Mid-II
16	Pipelining: An approach to optimize sequential circuits, Latch- vs. Register-Based Pipelines, NORA-CMOS—A Logic Style for Pipelined Structures	CO5	1. Explain NORA-CMOS logic for pipelined structure. 2. Discuss how to optimize a digital integrated circuit using pipelining with the help of an example.	Lecture/ Discussion	Assignment-II/Quiz-II/Mid-II
17	Non-Bistable Sequential Circuits: The Schmitt trigger, Monostable Sequential Circuits, Astable Circuits, Perspective: Choosing a Clocking Strategy.	CO5	1. Explain about Bistable and Nonbistable sequential circuits. 2. Write short notes on clock skew.	Lecture/ Discussion	Assignment-II/Quiz-II/Mid-II
18	Mid-Test 2	------	----------		
19/20	END EXAM	------	------		