SCHEME OF COURSE WORK

Course Title	:Digital IC Applications		
Course Code	:13EC1108	L T P C	4 1 0 3
Program:	:B.Tech		
Specialization:	: Electronics and Communication Engineering		
Semester	:IV		
Prerequisites	: Electronic Devices, Electronic Circuits, Switching Theory and Logic Design.		
Courses to which it is a prerequisite	:		

Course Outcomes (Cos):

1	Gain Knowledge on different logic families.
2	Analyze CMOS steady state and dynamic electrical behavior
3	Comprehend concepts of VHDL.
4	Design and model combinational and sequential logic circuits using VHDL.
5	Discuss internal structure, Read and Write timing operations of Memories.

Course Outcomes versus Program Outcomes:

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**S**	**M**	**M**	**S**								**M**
CO2	**S**	**M**	**M**	**M**								**M**
CO3			**M**		**S**							**M**
CO4	**S**		**M**		**M**							**M**
CO5			**M**		**M**							**M**

S - Strongly correlated, M - Moderately correlated, Blank - No correlation

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Week	Topic /Contents	Course Outcomes	Sample questions	Teaching-Learning Strategy	Assessment Method & Schedule
1	Introduction to logic families, CMOS logic.	CO1	1. Design a 4-input CMOS OR-AND-INVERT gate. Explain the circuit with the help of logic diagram and function table? 2. Design f = (A+BC)' using CMOS logic.	Lecture/ Design	Assignment I/Quiz-I/Mid-I
2	CMOS steady state and dynamic electrical behavior.	CO2	1. Derive the expressions for rise time and fall time of a CMOS inverter. 2. Analyze the fall time of CMOS inverter output with R_L = 100Ω, V_L = 2.5V and C_L =100PF. Assume V_L as stable state voltage.	Lecture/ Problem solving	Assignment I/Quiz-I/Mid-I
3	NMOS, PMOS, RTL, DCTL.	CO1	1. Design f = (A+BC)' using NMOS logic. 2. Design & Explain the operation of 2-input NAND gate using RTL.	Lecture/ Design/ Problem solving	Assignment I/Quiz-I/Mid-I
4	DTL, HTL, IIL.	CO1	1. Design & Explain the operation of 2-input NAND gate using DTL. 2. Explain the operation of inverter using IIL.	Lecture/ Problem solving	Assignment I/Quiz-I/Mid-I
5	TTL, Schottky TTL, Emitter coupled logic, Comparison of logic families.	CO1	1. Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation. 2. Compare CMOS, TTL and ECL with reference to logic levels, D.C noise margin, propagation delay and fan-out.	Lecture/ Problem solving	Assignment I/Quiz-I/Mid-I
6	CMOS logic families, CMOS/TTL interfacing, low voltage CMOS logic and interfacing, Familiarity with standard 74xx and CMOS 40xx series ICs-specifications.	CO2	1. What is interfacing? How it can be done. 2. Explain about low voltage CMOS logic and interfacing.	Lecture/ Problem solving	Assignment I/Quiz-I/Mid-I
7	Introduction to VHDL, Program structure, data types and constants, operators, data flow design elements	CO3	1. Write VHDL code for prime number detector using conditional signal assignment statement. 2. List out various data types of VHDL. Explain each one with example.	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
8	Behavioral design elements, Structural design elements, functions and procedures, libraries and packages, simulation and	CO3	1. List out various types of structural-flow design elements of VHDL. Explain any one with example. 2. Explain with example the syntax and the function of the following VHDL statements? (a) Process statement	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I

	synthesis.		(b) If, else and else if statements (c) Case statement (d) Loop statement		
9	Mid-Test-1	--	---------	------	----------
10	Decoders, encoders.	CO4	1. Design 5 to 32 decoder using 3 to 8 decoders. 2. Write behavioral VHDL program for a 74x148.	Lecture/ Design/ Programming	Assignment II/Quiz-II/Mid-II
11	Three state devices, Multiplexers and demultiplexers.	CO4	1. Design a 32 to 1 multiplexer using four 74×151 multiplexers and 74X139 decoder? Write a VHDL program for the Same in Structural flow style. 2. Design a 3 input 5 bit multiplexer. Write the truth table and draw the logic diagram. Provide the dataflow VHDL program of the same.	Lecture/ Design/ Programming	Assignment II/Quiz-II/Mid-II
12	Code Converters, Parity circuits, comparators.	CO4	1. Design and write VHDL code for 3 bit binary to gray code converter. 2. Design 8 bit comparator using 74x85 ICs. And write structural style VHDL code.	Lecture/ Design/ Programming	Assignment II/Quiz-II/Mid-II
13	Adders & subtractors, Basic Concepts of ALUs, Combinational multipliers.	CO4	1. Design a full adder using two half adders and write VHDL code for it using structural design modeling. 2. Design a 4×4 combinational multiplier and write the necessary VHDL program in data flow model.	Lecture/ Design/ Programming	Assignment II/Quiz-II/Mid-II
14	Barrel shifter, floating-point encoder, dual priority encoder.	CO4	1. Design a barrel shifter for 8-bit using three control inputs. Write a VHDL program for the same in data flow style. 2. Write VHDL code for fixed point to floating point conversion.	Lecture/ Design/ Programming	Assignment II/Quiz-II/Mid-II
15	Latches and flip-flops, PLDs, Counters, shift register.	CO4	1. Write VHDL code for JK F/F. 2. Write VHDL code for 4 bit shift register. 3. Design 4 bit up counter and write VHDL code.	Lecture/ Design/ Programming	Assignment II/Quiz-II/Mid-II
16	ROM - Internal structure, 2D-decoding commercial types, timing and applications.	CO5	1. What is ROM? Explain the internal ROM structure with logic diagram of 8x4 diode ROM. 2. Explain the commercial ROM types.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
17	Static RAM - Internal structure, SRAM timing, standard SRAMS, synchronous SRAMS, Dynamic RAM - Internal structure, timing, synchronous DRAMs.	CO5	1. Define timing parameters for Read operations in a static RAM with Timing diagram. 2. What is the difference between SRAM and DRAM.? Explain DRAM read – cycle Timing.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
18	Mid-Test 2	------	----------		
19/20	END EXAM	------	------		