SCHEME OF COURSE WORK

Course Details:

Course Title	: **DIGITAL DESIGN THROUGH VERILOG**		
Course Code	**: 13EC1132**	**L T P C**	**:4 0 0 3**
Program:	**: B.Tech.**		
Specialization:	**: Electronics and Communications Engineering**		
Semester	**: VII**		
Prerequisites	**:STLD**		
Courses to which it is a prerequisite	**: --**		

Course Outcomes (COs):

1	Describe the basic concepts of Verilog language.
2	Classify gate level modeling, dataflow level modeling and model digital circuits.
3	Distinguish behavioral level modeling, switch level modeling and model combinational, sequential circuits.
4	Differentiate Functions, Tasks, User defined primitives and design of an RTL models for memories and buses.
5	Identify Xilinx 3000 series FPGAs and Altera FLEX 10K series CPLDs.

Course Outcome Versus **Program Outcomes:**

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO 1	S	S		M	M							M
CO 2	S	S		S	S							M
CO 3	S	S		S	S							M
CO 4	S	S		M	S							M
CO 5	S	S		M	S							M

S - Strongly correlated, *M* - *Moderately* correlated, *Blank* - *No correlation*

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Teaching-Learning and Evaluation

Week	TOPIC / CONTENTS	Course Outcomes	Sample questions	TEACHING-LEARNING STRATEGY	Assessment Method & Schedule
1	**Introduction to Verilog:** Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools	CO-1	1.Briefly describe the basic modeling styles supported by Verilog HDL . 2. Define and explain the following terms relevant to Verilog HDL. 1. Module 2. Test bench	▫ Lecture ▫ Discussion ▫ Programming	Assignment I/Quiz-I / Mid 1
2	**Language constructs and conventions:** Test Benches. Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators.	CO-1	1.Explain about following Language constructs and conventions in Verilog. 1.Identifiers 2.Numbers 3.Strengths 4.Data types 5.Comments 2.What are the various data types available in Verilog HDL. Explain them with necessary syntax and suitable example.	▫ Lecture ▫ Discussion ▫ Programming	Assignment I/Quiz-I / Mid 1
3	**GATE LEVEL MODELING:** Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples.	CO-2	1. Implement the gate level description of a 2 to 4 decoder circuit with relevant logic diagram and Verilog HDL source code. 2. Implement gate level description of a 4 to 1 multiplexer circuit with relevant logic diagram and Verilog HDL source code.	▫ Lecture ▫ Discussion ▫ Programming	Assignment I/Quiz-I / Mid 1
4	**GATE LEVEL MODELING:** Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip-flops with Gate Primitives, programs.	CO-2	1. Design a 4 bit ALU which can perform the following functions. 1. Addition of two 4-bit numbers,2. Complementing all the bits of a 4-bit vector, 3. Bit by bit AND operation,4. Bit by bit XOR operation. Write Verilog HDL source code and draw the relevant synthesized circuits. 2.Implement the gate level description of a JK Flip flop.	▫ Lecture ▫ Discussion ▫ Programming	Assignment I/Quiz-I / Mid 1
5	**GATE LEVEL MODELING:** Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits, programs.	CO-2	1. Describe the following relevant to gate level modeling with necessary syntax and example. 1. Gate delays 2. Strengths and contention Resolution	▫ Lecture ▫ Discussion ▫ Programming	Assignment I/Quiz-I / Mid 1
6	**DATA FLOW LEVEL MODELING:** Introduction, Continuous Assignment	CO-2	1.Explain the operators in Verilog.	▫ Lecture ▫ Discussion ▫ Programming	Assignment I/Quiz-I /

	Structures, programs.		2.Write a Verilog HDL source code for 4-bit ALU using assign construct.		Mid 1
7	**DATA FLOW LEVEL MODELING:** Delays and Continuous Assignments, Assignment to Vectors, Operators, programs.	CO-2	1. Describe the continuous assignment feature of Verilog HDL with suitable example. 2. Write a Dataflow level description for a BCD adder	▫ Lecture ▫ Discussion ▫ Programming	Assignment I/Quiz-I / Mid 1
8	**BEHAVIORAL MODELING:** Introduction, Operations and Assignments, Functional Bifurcation, *Initial* Construct, *Always* Construct, Examples	CO-3	1.Implement the behavioral level description of a JK Flip flop circuit using an always statement and draw the synthesized circuit. 2. Implement the behavioral level description of a bi-directional shift register.	▫ Lecture ▫ Discussion ▫ Programming	Assignment I/Quiz-I / Mid 1
9	**Mid-Test 1**	CO-1,CO-2, CO3	----	----	----
10	**BEHAVIORAL MODELING:** Assignments with Delays, *Wait* construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-blocking Assignments, The case statement, Simulation Flow. I*f* and i*f*-else constructs	CO-3	1.Write a behavioral level description of 4-bit up/down counter. 2. Write a Verilog HDL source code for clocked RS flip flop and draw the relevant synthesized circuit along with simulation results.	▫ Lecture ▫ Discussion ▫ Programming	Assignment 2/Quiz-2 / Mid 2
11	**BEHAVIORAL MODELING:** assign-de assign construct, repeat construct, for loop, the disable construct, whileloop, forever loop, parallel blocks, force-release construct, Event.	CO-3	1. Explain different Loop statements with necessary syntax and relevant example. 2. Write about the following statements using (i)If statement (ii)Case statement (iii)Loop statement	▫ Lecture ▫ Discussion ▫ Programming	Assignment 2/Quiz-2 / Mid 2
12	**SWITCH LEVEL MODELING:** Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Tri reg Nets	CO-3	1. What are the various switch level primitives and give their instantiations .Draw the basic CMOS inverter circuit and write its Verilog HDL source code. 2. Write a switch level description for a 2 input NMOS NOR gate with active pull up load.	▫ Lecture ▫ Discussion ▫ Programming	Assignment 2/Quiz-2 / Mid 2
13	**Functions, Tasks and User-Defined Primitives:** Introduction, Function, recursive functions, Tasks, User- Defined Primitives (UDP)- combinational UDPs, sequential UDPs, FSM Design.	CO-4	1.Define User define primitives with syntax. Explain the difference between combinational and sequential UDP s with examples. 2. What is a State machine? Design a Moore machine for a sequence generator to sequence through eight distinct states.	▫ Lecture ▫ Discussion ▫ Programming	Assignment 2/Quiz-2 / Mid 2

			The states are represented by a set of four binary variables—W,X,Y,Z. The states and sequence are as follows(the four bits represent values of W<X<Y and Z respectively): 1000 → 1100 → 0100 →0110 →0010 →0011 →0001 →1001→1000→---		
14	**System Tasks, Functions, and Compiler Directives:** Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations.	CO-4	1. Explain about System Tasks in Verilog HDL 2. Write about standard compiler directives used in Verilog HDL	▫ Lecture ▫ Discussion ▫ Programming	Assignment 2/Quiz-2 / Mid 2
15	**Verilog models for memories and buses:** Static RAM Memory, A simplified 486 Bus Model, UART Design.	CO-4	1.Explain read & write cycle timing operations in static – RAM memory . 2.Design and write verilog HDL source code for 486 bus model.	▫ Lecture ▫ Discussion ▫ Programming ▫ PPT	Assignment 2/Quiz-2 / Mid 2
16	**Designing with field programmable gate arrays and complex programmable logic devices:** Xilinx 3000 Series FPGAs, Designing with FPGAs, Using a One-Hot State Assignment.	CO-5	1. Explain architecture of XILINX 3000 series FPGA. 2. Explain one-hot state assignment.	▫ Lecture ▫ Discussion ▫ Programming ▫ PPT	Assignment 2/Quiz-2 / Mid 2
17	Altera Complex Programmable Logic Devices(CPLDs), Altera FLEX 10K Series CPLDs.	CO-5	1.Explain the architecture of Altera FLEX 10K Series CPLD. 2.Discuss I/O block of Altera FLEX 10K Series CPLD	▫ Lecture ▫ Discussion ▫ Programming ▫ PPT	Assignment 2/Quiz-2 / Mid 2
18	**Mid-Test 2**	CO-3,CO-4, CO5	----	----	----
19/20	**END EXAM**				