SCHEME OF COURSE WORK

Course Title	: **CPLD AND FPGA ARCHITECTURE AND APPLICATIONS**		
Course Code	: 13EC2205	L T P C	4 0 0 3
Program:	:M.Tech		
Specialization:	: VLSI Design and Embedded systems		
Semester	:I		
Prerequisites	: Verilog/VHDL		
Courses to which it is a prerequisite	: Embedded Systems		

Course Outcomes (Cos):

1	Acquire Knowledge about various architectures and device technologies of PLD's
2	Comprehend FPGA Architectures
3	Describe FSM and different FSM techniques like petrinets & different case studies
4	Comprehends FSM Architectures and their applications.
5	Analyze System level Design and their application for Combinational and Sequential Circuits.

Course Outcomes versus Program Outcomes:

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1				M					M			M
CO2			M	M					M	M		M
CO3				M					M			M
CO4			M	M					M			S
CO5	**M**		M	S						M		S

S - Strongly correlated, M - Moderately correlated, Blank - No correlation

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Week	Topic /Contents	Course Outcomes	Sample questions	Teaching-Learning Strategy	Assessment Method & Schedule
1	ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices	CO1	1. differentiate PAL and PLA strustures 2. Realize nMOS switch 3. Realize the following nMOS PLA function F0= ∑ m(0,1,4,6)	Lecture	Assignment I/Quiz-I/Mid-I
2	Altera series – Max 5000/7000 series and Altera FLEX logic – 10000 series CPLD, AMD's – CPLD (Mach 1 to 5)	CO1	1.Draw CPLB structure of Altera Max 7000 2.What Is fan-in issue and how to minimize with an example	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
3	Cypres FLASH 370 Device Technology, Lattice LSI's Architectures – 3000 Series – Speed Performance and in system programmability.	CO1	1.Explain the Features of Cypress Logic Block 2. Give Architecture of LSI 3000 series	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
4	Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs	CO2	1.How to solve fan-in problem 2. explain segmented channel with an example	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
5	Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array):	CO2	1.Explain the Features of AT&T ORCA FPGA 2. Give Architecture of Xilinx 4000 FPGA	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
6	ACTEL's – ACT-1, 2,	CO3	1..Differentiate Actel		Assignment

	3 and their speed performance.		ACT1 and 3 2. What is the advantage of Flash based FPGA's	Lecture/ Problem solving	I/Quiz-I/Mid-I
7	Top Down Design – State Transition Table, state assignments for FPGAs Derivations of state machine charges .	CO2	1Draw the SMT of a Multiplier 2. What is a Linked state machine. Give an Example	Lecture/ Problem solving	Assignment I/Quiz-I/Mid-I
8	Realization of state machine charts with a PAL	CO3	1.Realize state machine with PAL	Lecture/ Problem solving	Assignment I/Quiz-I/Mid-I
9	Mid-Test 1	--		------	----------
10	Alternative realization for state machine chart using microprogramming	CO3	1.Realize SM chart with Microprogramming	Lecture/ Problem solving	Assignment II/Quiz-II/Mid-II
11	Linked state machines Petrinets for state machines – basic concepts, properties	CO3	1.What is live Petrinet. Give an example 2. Explain one hot encoding with an Example	Lecture/ Problem solving	Assignment II/Quiz-II/Mid-II
12	extendedpetrinets for parallel controllers.	CO3	1.What is unbounded petrinet give an example 2	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
13	Architectures centered around non-registered PLDs. State machine designs centered around shift registers.	CO4	1.What is Parallel in serial out shift register 2.Describe state machine design with shift registers	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
14	One – Hot design method. Use of ASMs in One – Hot design. Application of One – Hot method.	CO4	1.Explain one hot encoding with an Example 2.What is Metastability	Lecture/ Problem solving	Assignment II/Quiz-II/Mid-II
15	Controller, data path and functional partitions, Parallel	CO5	1.Give the Example of one to three pulse generator using PLA	Lecture/ Problem solving	Assignment II/Quiz-II/Mid-II

	adder cell		2. What are the Applications of One hot encoding Design a Parallel adder combinational circuit b.		
16	parallel adder sequential circuits, counters, multiplexers, parallel controllers.	CO5	1.Differentiate between combinational and Sequential Circuit 2. Design a Decade Counter	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
17	parallel adder sequential circuits, counters	CO5	1.What is Data Path and Control Path 2. Design a sequential circuit	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
18	Mid-Test 2	------			
19/20	END EXAM	------			