SCHEME OF COURSE WORK

Course Title	: Algorithms For VLSI Design Automation		
Course Code	:13EC2214	L P C	4 0 3
Program:	:M.Tech		
Specialization:	: VLSI Design and Embedded Systems		
Semester	:II		
Prerequisites	:VLSI Design		
Courses to which it is a prerequisite	:		

Course Outcomes (Cos):

1	Modify the CAD design problems using algorithmic paradigms
2	Illustrate Backend Design Concepts
3	Illustrate about Modeling and Simulation of Digital Circuits
4	Summarize about different Logic Synthesis and its verification
5	Analyze physical design problems of FPGA,MCM

Course Outcomes versus Program Outcomes:

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	**S**	**S**	**S**	**M**	**M**						**M**
CO2	**S**	**M**	**S**		**S**						**M**
CO3	**S**				**S**						**M**
CO4	**S**	**S**	**M**	**S**	**M**						**M**
CO5	**S**	**S**	**M**	**M**	**M**						**M**

S - Strongly correlated, M - Moderately correlated, Blank - No correlation

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Week	Topic /Contents	Course Outcomes	Sample questions	Teaching-Learning Strategy	Assessment Method & Schedule
1	Introduction to Design Methodologies, Design Automation tools,	CO1	1. What are the important entities for VLSI Design? 2 Draw the sketch of Gajskis' Y-chart and explain about the visualization of the three design domains.	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
2	Algorithmic Graph Theory Computational Complexity, Tractable and Intractable Problems	CO1	1. Explain how a Depth-first search algorithm is used to reduce the computational Complexity 2. With the help of Psuedo Code explain Prim's Algorithm for Spanning Trees	Lecture/ Problem Solving/ Algorithm	Assignment I/Quiz-I/Mid-I
3	General Purpose Methods for Combinational Optimization: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search,	CO1	1. Give an algorithm for an exhaustive search by means of back tracking 2.Write an algorithm for branch and bound method.	Lecture/ Algorithm	Assignment I/Quiz-I/Mid-I
4	Simulated Annealing, Tabu search, Genetic Algorithms. LAYOUT COMPACTION: Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint –graph Compaction.	CO1,CO2	1. Give pseudo code description of simulated annealing. 2. Explain how a genetic Algorithm is used for search & solution of a given Problem? 3.Explain about Liao-Wang Algorithm	Lecture/ Algorithm	Assignment I/Quiz-I/Mid-I
5	Placement and Partitioning: Circuit	CO2	1.Explain about Kernighan-Lin	Lecture/ Algorithm	Assignment I/Quiz-I/Mid-I

	Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithms, Partitioning		Partioning Algorithm 2.Explain about Placement Algorithm		
6	Floor Planning: Floor Planning Concepts, Shape Functions and Floor plan Sizing	CO2	1.Explain about the terminology of Floor Planning 2.Explain about Optimization problems of Floor Planning	Lecture/ Discussion	Assignment I/Quiz-I/Mid-I
7	Routing: Types of Local Routing Problems, Area Routing, Channel Routing	CO2	1.With the help of Psuedo Code explain Area Routing Algorithm 2. With the help of Psuedo Code explain Channel Routing Algorithm	Lecture/ Algorithm	Assignment I/Quiz-I/Mid-I
8	Introduction to Global Routing, Algorithms for Global Routing	CO2	1.Describe Global Routing and how it is represented in Layout Form	Lecture/ Algorithm	Assignment I/Quiz-I/Mid-I
9	Mid-Test-1	CO1,CO2			
10	MODELLING AND SIMULATION: Gate Level Modeling and Simulation,	CO3	1.What is meant by modeling and simulation? 2.Explain Compiler Driven Simulation	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
11	Switch level modeling and simulation LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology,	CO3,CO4	1.Differentiate gate level and switch level modeling and simulation procedures with suitable example. 2. Describe the basic issues and terminology employed in logic synthesis in VLSI design.	Lecture/ Algorithm	Assignment II/Quiz-II/Mid-II
12	Binary –Decision diagram, Two – Level Logic	CO4	1. Explain about binary-decision diagrams with an	Lecture/ Algorithm	Assignment II/Quiz-II/Mid-II

	Synthesis.		example. 2.Explain about two level logic synthesis with suitable example.		
13	High Level Synthesis: Hardware Models, Internal representation of the input algorithm, Allocation, Assignment and Scheduling,	CO4	1. With an example explain how high level transformations can be carried out on Data Flow Graphs. What are the advantages and limitations? 2.Explain about Allocation, Assignment and Scheduling of Algorithms in high-level synthesis.	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
14	Some Scheduling Algorithms, Some aspects of Assignment problem, High – level Transformations.	CO4	1.Explain about optimization issues in High-level synthesis. 2.Explain about high level transformations related to high level synthesis.	Lecture/ Algorithm	Assignment II/Quiz-II/Mid-II
15	FPGA technologies, Physical Design cycle for FPGA's partitioning and routing for segmented and staggered models.	CO5	1.Give the physical Design cycle for FPGAs and explain about the same 2.Describe the routing Algorithm for staggered model and compare it with Segmentation model.	Lecture/ Algorithm	Assignment II/Quiz-II/Mid-II
16	Physical Design Automation of MCM's: MCM technologies, MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches,	CO5	1. What are the various steps in MCM physical design cycle? Explain them briefly. 2. How MCM partioning is carried out? Explain with the help of a system graph	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II

17	Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, routing and programmable MCM's.	CO5	1.Explain briefly about Multiple Stage Routing Algorithms in MCM 2.Explain about Maze Routing	Lecture/ Discussion	Assignment II/Quiz-II/Mid-II
18	Mid-Test 2	CO3,CO4, CO5			
19/20	END EXAM	COs 1 to5			