SCHEME OF COURSE WORK

Course Details:

Course Title	: **ANALOG IC DESIGN**		
Course Code	**: 13EC2210**	**L T P C**	**:4 0 0 3**
Program:	**: M.Tech.**		
Specialization:	**: VLSI Design and Embedded Systems**		
Semester	**: II**		
Prerequisites	**:EDC,LICA**		
Courses to which it is a prerequisite	**: --**		

Course Outcomes (COs):

1	Analyze small signal modeling of single stage MOSFET amplifiers with current mirrors.
2	Design two stage CMOS operational amplifiers.
3	Illustrate advanced current mirrors and comparators.
4	Outline concepts of sample& Hold circuits and switched capacitor circuits.
5	Design and analyze CMOS A/D and D/A data converters of different types.

Course Outcome Versus **Program Outcomes:**

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO-1	S	S		S	S				M		
CO-2	S	S		S	S				M		
CO-3	S	S		S	S				M		
CO-4	S	S		S	S				M		
CO-5	S	S		S	S				M		

S - Strongly correlated, *M - Moderately* correlated, *Blank - No correlation*

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Teaching-Learning and Evaluation

Week	TOPIC / CONTENTS	Course Outcomes	Sample questions	TEACHING-LEARNING STRATEGY	Assessment Method & Schedule
1	MOS MODELING AND CURRENT MIRRORS: Large Signal and Small Signal Modeling of MOSFET, Advanced MOS Modeling	CO-1	1. Explain small signal modelling of MOS Transistor in the active region and derive the expressions for trans conductance ,Body effect Conductance and finite output impedance. 2. Explain Small Signal Capacitances for an n-channel MOS transistor	▫ Lecture ▫ Discussion	Mid1/Assignment 1
2	**MOS MODELING AND CURRENT MIRRORS:** Simple CMOS Current Mirror, Common Source,	CO-1	1.Draw the circuit and small signal model for simple CMOS current mirror and explain.	▫ Lecture ▫ Discussion	Mid1/Assignment 1

	Common Drain, Common Gate amplifiers		2. Derive the expressions for input resistance and gain of Common Gate Amplifier with a current mirror active load.		
3	**MOS MODELING AND CURRENT MIRRORS:** Source degenerated current mirrors, High Output Impedance Current Mirrors, cascade gain stage, MOS Differential pair and gain stage, frequency response.	CO-1	1. Explain High output impedance current mirrors and derive the expressions for output impedance. 2.Draw the small signal model of differential input single ended output MOS gain stage and derive gain of the amplifier.	▫ Lecture ▫ Discussion	Mid1/Assignment 1
4	**BASIC OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION:** Two Stage CMOS Operational Amplifier, opamp gain, frequency response, slew rate, systematic offset voltage, Feedback and Operational Amplifier Compensation-linear settling time.	CO-2	1. Draw the circuit for CMOS two-stage op-amp and derive the expression for Gain. 2. Derive the expressions for Unity gain frequency and slew rate of a Two Stage Opamp.	▫ Lecture ▫ Discussion	Mid1/Assignment 1
5	**BASIC OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION:** Test opamp compensation, compensating the two stage opamp, lead compensation, compensation independent of process and temperature.	CO-2	1. Draw the small signal model of two stage opamp and discuss how a two stage opamp can be compensated. 2. Derive gain and linear settling time for first order model of closed loop amplifier.	▫ Lecture ▫ Discussion	Mid1/Assignment 1
6	**ADVANCED CURRENT MIRRORS & COMPARATORS:** Advanced Current Mirrors, Folded-Cascode Operational Amplifier, Current Mirror Operational Amplifier	CO-3	1.Explain wide swing cascode current mirror with enhanced output impedance. 2.Explain the Small Signal analysis of Folded cascode Opamp.	▫ Lecture ▫ Discussion ▫ PPT	Mid1/Assignment 1
7	**ADVANCED CURRENT MIRRORS & COMPARATORS:** Linear settling time revisited, Fully Differential Operational Amplifiers.	CO-3	1. Explain fully differential folded cascode opamp. 2. Discuss how to generate 3db frequency of a closed loop amplifier.	▫ Lecture ▫ Discussion ▫ PPT	Mid1/Assignment 1
8	**ADVANCED CURRENT MIRRORS & COMPARATORS:** Common Mode Feedback Circuits, Current Feedback Operational Amplifier.	CO-3	1. Draw the circuit and explain modified Common mode feedback circuit. 2.Explain current feedback opamp using Wilson current mirror.	▫ Lecture ▫ Discussion ▫ PPT	Mid1/Assignment 1
9	**Mid-Test 1**	CO-1 , CO2,CO-3	----------	---------	----
10	**ADVANCED CURRENT MIRRORS & COMPARATORS:** Comparators: using an opamp for a comparator, Charge Injection Error, Latched Comparators, CMOS and Bi CMOS Comparators.	CO-3	1. Discuss the architecture of latched comparator. 2. Explain the typical architecture of a high speed comparator.	▫ Lecture ▫ Discussion ▫ PPT	Mid2 /Assignment 2
11	**SAMPLE AND HOLD &SWITCHED CAPACITOR CIRCUITS:** Sample & Hold Circuits: Performance of Sample & Hold Circuit,MOS Sample and Hold Circuits.	CO-4	1. Discuss the test setup for characterizing a sample and hold using a beat test. 2. Discuss an open loop sample and	▫ Lecture ▫ Discussion ▫ PPT	Mid2 /Assignment 2

			hold realization using transmission gates for clock feed through cancellation		
12	**SAMPLE AND HOLD &SWITCHED CAPACITOR CIRCUITS:** CMOS, BiCMOS Sample and Hold Circuits.	CO-4	1. Explain a bipolar track and hold based on diode bridge. 2.Discuss a simple non inverting sample and hold circuit with clock feed through cancellation.	▫ Lecture ▫ Discussion ▫ PPT	Mid2 /Assignment 2
13	**SAMPLE AND HOLD &SWITCHED CAPACITOR CIRCUITS:** Switched Capacitor Circuits: Basic Operation and Analysis, First Order and Biquard Filters, Charge Injection	CO-4	1. Explain a High-Q Switched Capacitor Biquad Filter and derive transfer function 2. Draw the diagram of parasitic sensitive integrator and derive the expression for transfer function.	▫ Lecture ▫ Discussion ▫ PPT	Mid2 /Assignment 2
14	**SAMPLE AND HOLD &SWITCHED CAPACITOR CIRCUITS:** Switched CapacitorGain Circuit, Correlated Double Sampling Techniques. Other Switched Capacitor Circuits.	CO-4	1. Explain Resettable Switched Capacitor Gain circuit and derive the expression for output voltage. 2. Discuss other type of switched capacitor circuits useful for non linear applications.	▫ Lecture ▫ Discussion ▫ PPT	Mid2 /Assignment 2
15	**NYQUIST RATE D/A &A/D CONVERTERS:** Introduction to ideal data converters, Quantization Noise, Performance Limitations	CO-5	1. Explain the term Quantization noise .Derive the RMS value of the noise signal, $V_{Q(rms)}$ for a ramp signal. 2. Explain ideal A/D Converter and draw input-output transfer curve for a2-bit A/D converter.	▫ Lecture ▫ Discussion ▫ PPT	Mid2 /Assignment 2
16	**NYQUIST RATE D/A &A/D CONVERTERS:** Nyquist rate D/A converters: Decoders Based Converters, Binary Scaled Converters, Thermometer-code converters, Hybrid Converters.	CO-5	1. Design a 4-bit R-2R based D/A converter and derive the expression for output voltage. 2.Explain the operation of 15 bit resistor capacitor hybrid data converters	▫ Lecture ▫ Discussion ▫ PPT	Mid2 /Assignment 2
17	**NYQUIST RATE D/A &A/D CONVERTERS:** Nyquist rate A/D converters: Integrating, Successive Approximation, Cyclic, Flash Type, Two Step, Interpolating, Folding, Pipelined A/D Converters.	CO-5	1. Draw the schematic for MOS successive approximation type ADC and explain its working. 2. Draw the schematic of 3bit Flash A/D converter and discuss the design issues.	▫ Lecture ▫ Discussion ▫ PPT	Mid2 /Assignment 2
18	**Mid-Test 2**	CO-3,CO-4,CO5	**----------**	**----------**	------
19/20	**END EXAM**				