SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE – I)

Course Code: 13EC2206 **L P C**
4 0 3

Course Outcomes

At the end of the course the student will be able to

CO1: Comprehend abstraction in Hardware, SOC of ARM Processor.

CO2: Evaluate and analyze system on chip RISC Machine, 3and5 stage Pipeline.

CO3: Develop programs on ARM Processor.

CO4: Explain Memory Hierarchy ARM Interface.

CO5: Integrate the Knowledge of ARM for applications of System on Chip.

UNIT-I

INTRODUCTION TO PROCESSOR DESIGN:

Abstraction in hardware design, MUO a simple processor, Processor design trade off, Design for low power consumption.

UNIT-II

ARM PROCESSOR AS SYSTEM-ON-CHIP:

Acorn RISC Machine – Architecture inheritance –ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM Co-processor interface.

UNIT-III

ARM ASSEMBLY LANGUAGE PROGRAMMING:

ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – co-processor instructions.

Architectural Support for High Level Language - Data types – Abstraction in software design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory.

UNIT-IV

MEMORY HIERARCHY:

Memory size and speed –on chip memory –caches-cache design an example-Memory management

Architectural Support for System Development-Advanced Microcontroller bus architecture-ARM Memory Interface-ARM Reference Peripheral specification –Hardware System Prototyping tools – Emulator –Debug architecture

UNIT-V

ARCHITECTURAL SUPPORT FOR OPERATING SYSTEM:

An introduction to Operating Systems-ARM System Control coprocessor-CP15 Protection unit registers-ARM protection unit-CP15 MMU registers-ARM Architecture-Synchronization-Context Switching input and output

TEXT BOOKS:

[1] Steve Furber, "*ARM system on chip Architecture*", 2nd ed., Addison Wesley Professional, 2000.

REFERENCES:

[1] Michael J Flynn,Wayne Luck, "*Computer System Design: System onChip*", Wiley India Edition.

[2] PrakashRashinkar, Peter Paterson and Leena Singh L., "*System on Chip Verification – Methodologies and Techniques*", Kluwer Academic Publisher, 2001.

[3] Ricardo Reis, "*Design of System on a Chip: Devices and Components*" 1st ed., Springer, 2004.