

LOW POWER VLSI DESIGN**Course Code: 13EC2211****L P C
4 0 3****Course Outcomes:**

At the end of the course the student will be able to

CO1: Illustrate the Design limitations of Low Power Design and Evolution of SOI Technologies.

CO2: Describe various integration and isolation techniques for MOS/Bi-CMOS Technologies.

CO3: Obtain Proficiency in parameter extraction of Bi-polar, MOSFETs using SPICE and Advanced MOSFET models.

CO4: Design and analyze Conventional CMOS and Bi-CMOS Logic Gates

CO5: Design low voltage, low power Bi-CMOS logic circuits to achieve High Performance.

UNIT- I**INTRODUCTION TO LOW POWER DESIGN:**

Introduction, Low Power design- an overview, low power design limitations: power supply voltage, threshold voltage, scaling, interconnect wires, Silicon-on-Insulator (SOI) From Devices to Circuits.

UNIT-II**MOS/BI-CMOS PROCESS TECHNOLOGY AND INTEGRATION:**

The Realization of Bi-CMOS processes, Bi-CMOS manufacturing and Integration Considerations, Isolation in Bi-CMOS, Deep submicron processes, Future trends and directions of CMOS/Bi-CMOS processes.

UNIT-III**DEVICE BEHAVIOR AND MODELING:**

The MOS (FET) Transistor, The Bipolar (Junction) transistor, MOSFET SPICE models, Advanced, Bipolar Spice models, MOSFET

in Hybrid Mode Environment-Surface p-Channel for Sub-Half-Micron Devices, Device Fabrication, Model Parameters Extraction, Sub-Half-Micron D.C. Model Formulation.

UNIT-IV

CONVENTIONAL CMOS AND BI-CMOS LOGIC GATES:

Conventional CMOS Logic Gates, Conventional Bi-CMOS Logic Gate, Bi-CMOS Circuits Utilizing Lateral pnp BJTs in pMOS structures, Performance evaluation and Comparison.

UNIT-V

LOW- VOLTAGE, LOW POWER LOGIC CIRCUITS:

Merged Bi-CMOS digital circuits, Full-Swing Multidrain/Multicollector Complementary Bi-CMOS Buffers, Quasi-Complementary Bi-CMOS Digital Circuits, Full-Swing Bi-CMOS/Bi-NMOS Digital circuits employing Schottky Diodes, Feedback-Type Bi-CMOS Digital Circuits, High-Beta Bi-CMOS Digital Circuits, Transiently Saturated Full-Swing Bi-CMOS Digital Circuits, Bootstrapped-type Bi-CMOS Digital circuits, ESD-free Bi-CMOS Digital circuit -circuit operation and comparative Evaluation.

Evolution of Latches and Flip-Flops, Quality measures for Latches and Flip-Flops, Design perspective.

TEXT BOOK:

- [1] KiatSeng Yeo, Samir S. Rofail, Wang-Ling Goh, "*CMOS/Bi CMOS ULSI Low Voltage Low Power*", Pearson Education Asia 1st Indian reprint, 2002.

REFERENCE BOOKS:

- [1] J.Rabaey, "*Digital Integrated Circuits*", PH. N.J 1996, 2nd Edition.
- [2] Sung-mokang and yusufleblebici, "*CMOS Digital ICs*", TMH, 3rd edition, 2003.
- [3] Parhi, "*VLSI DSP Systems*", John Wiley & sons, 2003 Reprint.
- [4] IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.