# ELECTRONIC DESIGN AUTOMATION TOOLS (ELECTIVE – II)

**Course Code: 13EC2213** **L P C**
**4 0 3**

**Course Outcomes:**

At the end of the course the student will be able to

CO1: Illustrate different simulations and delay models which are available for HDL.

CO2: Classify the different synthesis using CAD tools.

CO3: Design and analyze Analog And Digital Circuits Using PSPICE model of Transistor.

CO4: Describe about Analog, Digital & Mixed Signal Simulators.

CO5: Illustrate PCB Design and also describe the tools used for PCB design.

**UNIT-I**
**SIMULATION USING HDLS:**
Simulation-Types of Simulation, Logic Systems, Working of Logic Simulation, Cell Models, Delay Models, State Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation.

**UNIT-II**
**SYNTHESIS USING HDLS:**
Verilog and Logic Synthesis, VHDL and Logic Synthesis, Memory Synthesis, FSM Synthesis, Memory Synthesis, Performance-Driven Synthesis.
CAD Tools for Simulation and Synthesis: Modelsim and Leonardo Spectrum

**UNIT-III**
**CIRCUIT DESIGN AND SIMULATION USING PSPICE:**
Pspice Models For Transistors, A/D & D/A Sample And Hold Circuits etc., and Digital System Building Blocks, Design and Analysis of Analog and Digital Circuits Using PSPICE.

**UNIT-IV**

**AN OVERVIEW OF MIXED SIGNAL VLSI DESIGN:**

Fundamentals Of Analog And Digital Simulation, Mixed Signal Simulator Configurations, Understanding Modeling, Integration To CAD Environments.

**UNIT-V**

**TOOLS FOR PCB DESIGN AND LAYOUT:**

An Overview of High Speed PCB Design, Design Entry, Simulation and Layout Tools for PCB, Introduction to Orcad PCB Design Tools.

**TEXTBOOKS:**

[1] J.Bhaskar, "*A Verilog Primer*", BSP, 2003.

[2] J.Bhaskar, "*A Verilog HDL Synthesis*", BSP, 2003.

[3] M.H.RASHID, "*SPICE FOR Circuits and Electronics Using PSPICE*", (2/E) (1992) Prentice Hall.

**REFERENCE BOOKS:**

[1] ORCAD: Technical Reference Manual, Orcad, USA.

[2] SABER, "*Technical Reference Manual*", Analogy Nic, USA.

[3] M.J.S.SMITH, "*Application-Specific Integrated Circuits*", (1997). Addison Wesley.

[4] J.Bhaskar, "*A VHDL Synthesis Primer*", BSP, 2003.