DIGITAL DESIGN THROUGH HDL

Course Code: 13EC2203 **L P C**
4 0 3

Course Outcomes:

At the end of the Course, Students will be able to:

CO1: Distinguish dataflow, behavioral and structural design elements in VHDL.

CO2: Outline the basic concepts of Verilog language.

CO3: Classify gate level modeling and dataflow level modeling.

CO4: Distinguish behavioral level modeling and switch level modeling.

CO5: Design Finite state machines and comprehend concepts of functions, tasks, and user defined primitives.

UNIT-I
COMBINATIONAL AND SEQUENTIAL LOGIC DESIGN USING VHDL:
Data flow design elements, behavioral design elements, Structural design elements, simulation and synthesis, decoders, multiplexers, comparators, ALUs. Latches and flip-flops, counters, shift registers.

UNIT-II INTRODUCTION TO VERILOG:
Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches. Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators. System Tasks, Functions, and Compiler Directives: Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations.

UNIT-III GATE LEVEL MODELING:
Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip-flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits.

DATA FLOW LEVEL MODELING:
Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators.

UNIT-IV
BEHAVIORAL MODELING:
Introduction, Operations and Assignments, Functional Bifurcation, *Initial* Construct, *Always* Construct, Examples, Assignments with Delays, *Wait* construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-blocking Assignments, The case statement, Simulation Flow. I*f* and i*f*-else constructs, assign-deassignconstruct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.
SWITCH LEVEL MODELING:
Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets.

UNIT V
FUNCTIONS, TASKS AND USER-DEFINED PRIMITIVES:
Introduction, Function, recursive functions, Tasks, User- Defined Primitives (UDP)- combinational UDPs, sequential UDPs,
FSM DESIGN:
Moore and Mealy Machines.

TEXT BOOKS:
[1] John F.Wakerly, "*Digital Design Principles &Practices*", PHI/Pearson Education Asia, 3rd Ed., 2005.
[2] T.R.Padmanabhan and B.Bala Tripura Sundari, "*Design through Verilog HDL*", WSE, 2004 IEEE Press.

REFERENCE BOOKS:
[1] J.Bhasker, "*VHDL Primer*", Pearson Education/PHI, 3rd edition.
[2] MichaelD.Ciletti, "*Advanced Digital Design with Verilog HDL*", PHI, 2005.