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**DIGITAL IC DESIGN****Course Code: 13EC2212****L P C  
4 0 3****Course Outcomes:**

At the end of the course the student will be able to

CO1: Analyze the depth of designing a Digital IC and use the concept of logical effort for Transistor sizing.

CO2: Obtain Proficiency in SPICE modeling of CMOS circuits.

CO3: Describe the various design entities.

CO4: Distinguish between Static CMOS design and Dynamic CMOS design.

CO5: Design Logic gates, Flip-flops, Adders, Registers and RAM etc.

**UNIT-I INTRODUCTION:**

Historical Perspective, Issues in Digital Integrated Circuit Design, Quality Metrics of a Digital Design: Cost of an Integrated Circuit, Functionality and Robustness, Performance, Power and Energy Consumption.

**UNIT-II MOS TRANSISTOR:**

The MOS Transistor under Static Conditions, Dynamic Behavior, The Actual MOS Transistor—Some Secondary Effects, SPICE Models for the MOS Transistor, Method of Logical Effort for transistor sizing.

**WIRE:**

Introduction, A First Glance, Interconnect Parameters - Capacitance, Resistance, and Inductance, Electrical wire models, SPICE wire models.

**UNIT-III THE CMOS INVERTER:**

Introduction, The Static CMOS Inverter — An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Switching Threshold, Noise Margins, Robustness Revisited, Performance of CMOS Inverter: The Dynamic Behavior,

Computing the Capacitances, Propagation Delay: First-Order Analysis, Propagation Delay from a Design Perspective, Power, Energy, and Energy-Delay: Dynamic Power Consumption, Static Consumption, Perspective: Technology Scaling and its Impact on the Inverter Metrics .

#### UNIT-IV

##### **DESIGNING COMBINATIONAL LOGIC GATES IN CMOS:**

Introduction, Static CMOS Design: Complementary CMOS, Ratioed Logic, Pass-Transistor Logic, Dynamic CMOS Design: Dynamic Logic- Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Perspectives: How to Choose a Logic Style, Designing Logic for Reduced Supply Voltages

##### **UNIT-V DESIGNING SEQUENTIAL LOGIC CIRCUITS:**

Introduction, Timing Metrics for Sequential Circuits, Classification of Memory Elements, Static Latches and Registers: The Bistability Principle, Multiplexer-Based Latches Master-Slave Edge-Triggered Register, Low-Voltage Static Latches, Static SR Flip-Flops—Writing Data by Pure Force, Dynamic Latches and Registers: Dynamic Transmission-Gate Edge-triggered Registers ,C<sup>2</sup>MOS—A Clock-Skew Insensitive Approach, True Single-Phase Clocked Register (TSPCR). Pipelining: An approach to optimize sequential circuits, Latch- vs. Register-Based Pipelines, NORA-CMOS—A Logic Style for Pipelined Structures, Non-Bistable Sequential Circuits: The Schmitt trigger, Monostable Sequential Circuits, Astable Circuits, Perspective: Choosing a Clocking Strategy.

##### **TEXT BOOKS:**

- [1] Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, “*Digital Integrated Circuits – A design perspective*”, Second Edition, PHI, 2003.
- [2] S. M. Kang & Y. Leblebici, “*CMOS Digital Integrated Circuits*”, Third Edition, McGraw Hill, 2003.

##### **REFERENCES:**

- [1] Jackson & Hodges, “*Analysis and Design of Digital Integrated circuits*”. 3rd Ed. TMH Publication, 2005.
- [2] Ken Martin, “*Digital Integrated Circuit Design*”, Oxford Publications, 2001.
- [3] Sedra and Smith, “*Microelectronic Circuits*” 5/e, Oxford Publications, 2005.