
**ALGORITHMS FOR VLSI DESIGN AUTOMATION
(ELECTIVE – II)****Course Code: 13EC2214****L P C
4 0 3****Course Outcomes:**

At the end of the course the student will be able to

CO1: Modify the CAD design problems using algorithmic paradigms

CO2: Illustrate Backend Design Concepts

CO3: Illustrate about Modeling and Simulation of Digital Circuits

CO4: Summarize about different Logic Synthesis and its verification

CO5: Analyze physical design problems of FPGA,MCM

UNIT-I**PRELIMINARIES & GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION:**

Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems

General Purpose Methods for Combinational Optimization:

Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT-II**LAYOUT COMPACTION:**

Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint –graph Compaction.

Placement and Partitioning:

Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithms, Partitioning

Floor Planning:

Floor Planning Concepts, Shape Functions and Floor plan Sizing

Routing:

Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing

UNIT-III**MODELLING AND SIMULATION:**

Gate Level Modeling and Simulation, Switch level modeling and simulation

UNIT-IV**LOGIC SYNTHESIS AND VERIFICATION:**

Basic issues and Terminology, Binary –Decision diagram, Two – Level Logic Synthesis.

High Level Synthesis: Hardware Models, Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High – level Transformations.

UNIT-V**PHYSICAL DESIGN AUTOMATION OF FPGA'S AND MCM'S:**

FPGA technologies, Physical Design cycle for FPGA's partitioning and routing for segmented and staggered models.

Physical Design Automation of MCM's:

MCM technologies, MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin –Distribution and routing, routing and programmable MCM's.

TEXT BOOKS:

- [1] S.H.Gerez, “*Algorithms for VLSI Design Automation*”, WILEY student edition, John wiley& Sons (Asia) Pvt.Ltd. 1999.
- [2] NaveedSherwani, “*Algorithms for VLSI Physical Design Automation*”, Springer International Edition 3rd edition, , 2005

REFERENCES:

- [1] Hill & Peterson, “*Computer Aided Logical Design with Emphasis on VLSI*”, John Wiley, 1993.
- [2] Wavne Wolf, “*Modern VLSI Design: Systems on silicon*”, Pearson Education Asia, 2ND Edition, 1998.