COMPUTER ORGANIZATION AND ARCHITECTURE

Course Code: 13CS2102 **L P C**
4 0 3

Pre requisites: Advanced Computer Architecture

Course Outcomes:

At the end of the course, a student will be able to:

CO1 : Identify and apply the usage of instruction set characteristics, data types, addressing modes for designing current processors like ARM and describe the overview of computer organization.

CO2 : Apply knowledge on RISC, CISC processors, ARM and x86 processor family

CO3 : Associate with the Cache Memory mapping techniques and explain I/O organization.

CO4 : Enhance their perspective of modern computer system with pipelining, Vector Processing and super scalar processors.

CO5 : Gain proficiency in identifying the use of new concepts Multicore computers and can apply this knowledge on developing new applications.

UNIT - I

Overview of computer organization: Introduction, Programmer's view, Architect's view, Implementer's view, Te processor, Memory, Input/output. (Text Book 2)

Instruction Sets: Machine Instruction Characteristics, Types of Operands, Intel X86 and ARM Data Types, Types of Operations, Intel X86 and ARM Operation Types, Addressing, x86 and ARM Addressing Modes, Instruction Formats, x856 and ARM Instruction Formats, Assembly Language. (Text Book1)

UNIT – II

Processor Structure and Function: Processor Organization, Register Organization, The Instruction Cycle, The x86 Processor Family, The ARM Processor. (Text Book1)

RISC Processors: Introduction, Evolution of CISC Processors, RISC Design Principles. (Text Book2)

UNIT – III

Cache Memory: Introduction, How Cache Memory Works, Why Cache Memory Works, Cache Design Basics, Mapping Function, Replacement Policies, Write Policies, Space Overhead, Mapping Examples, Types of Cache Misses, Types of Caches.

Input/Output Organization: Accessing I/O Devices, I/O data Transfer, External Interface, Universal Serial Bus. (Text Book2)

UNIT – IV

Pipelining and Vector Processing: Basic Concepts, Handling Resource Conflicts, Data Hazards, Handling Branches, Performance Enhancements, Pentium Implementation, Vector Processors, Performance. (Text Book2)

Instruction-Level Parallelism and Superscalar Processors: Overview, Design Issues, Pentium4, ARM Cortex-A8. (Text Book1)

UNIT – V

Parallel Processing: The Use of Multiple Processors, Symmetric Multiprocessors, Cache Coherence and the MESI protocol, Multithreading and Chip Multiprocessors, Clusters, Non Uniform Memory Access Computers, Vector Computation. (Text Book1)

Multicore Computers: Hardware Performance Issues, Software Performance Issues, Multicore Organization, Intel x86 Multicore Organization, ARM11 MPCore. (Text Book1)

Text Books:

1. William Stallings, "Computer Organization and Architecture Designing for Performance", 8th Edition, Pearson Education, 2010.
2. Sivarama P.Dandamudi, "Fundamentals of Computer Organization and Design", International Edition, Springer ,2009.

References:

1. Moris Mono , "Computer System Architecture", 3rd Edition, Pearson / PHI, 1993.
2. Hamacher, Vranesic, Zaky , "Computer Organization", 5th Edition, TMH, 2002.
3. John D. Carpinelli , "Computer systems organization and architecture", 1st Edition, Pearson,2001.
4. Pal Chowdary , "Computer organization and Design", 2nd Edition, PHI, 2004.
5. Naresh Jotwani , "Computer system organization", 1st Edition, TMH, 2009.