SCHEME OF COURSE WORK

Course Title	Digital Electronics		
Course Code	22EE1107	L T P C	3 0 0 3
Program:	B.Tech.		
Specialization:	Electrical and Electronics Engineering		
Semester	IV		
Prerequisites	Electronic Devices and Analog Circuits		
Courses to which itis a prerequisite	Microprocessors and Microcontrollers		

Course Outcomes (COs):

CO-1	Explain Conversion of number from one number system to another Number system.
CO-2	Implement logic circuits using basic Logic gates or universal Logic gates and simplify logic expressions using basic theorems, K-map and Tabular method.
CO-3	Design combinational circuits using logic gates and Realize logic expressions using MUX, Decoder and PLDs.
CO-4	Analyze the design aspects of sequential circuits using flipflops and differentiate Mealy & Moore type Sequential machines.
CO-5	Explain digital logic families and their characteristics.

Program Outcomes (POs):
A graduate of B.Tech will be able to

PO 1	Apply the knowledge of basic sciences and electrical and electronics engineering fundamentals to solve the problems of power systems and drives.
PO 2	Analyze power systems that efficiently generate, transmit and distribute electrical power in the context of present Information and Communications Technology.
PO 3	Design and develop electrical machines and associated controls with due considerations to societal and environmental issues.
PO 4	Design and conduct experiments, analyze and interpret experimental data for performance analysis.
PO 5	Apply appropriate simulation tools for modeling and evaluation of electrical systems.
PO 6	Apply the electrical engineering knowledge to assess the health and safety issues and their consequences.
PO 7	Demonstrate electrical engineering principles for creating solutions for sustainable development.
PO 8	Develop a techno ethical personality that help to serve the people in general and Electrical and Electronics Engineering in particular.
PO 9	Develop leadership skills and work effectively in a team to achieve project objectives.
PO10	Communicate effectively in both verbal and written form.
PO11	Understand the principles of management and finance to manage project in multi-disciplinary environments.
PO12	Pursue life-long learning as a means of enhancing the knowledge and skills.

Course Outcomes versus Program Outcomes:

Cos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3											
CO2	3	2	2		2							3
CO3	3	2	2		2		2	2				3
CO4	3	2	2		2		2	2				3
CO5	3	2	2		2		2	2				3

3 - Strongly correlated, 2 - Moderately correlated, 1- Weakly correlated, Blank - No correlation

Assessment Methods:	Assignment / Quiz / Seminar / Case Study / Mid-Test / End Exam

Week	Topic /Contents	Course Outcomes	Sample questions	Teaching-Learning Strategy	Assessment Method & Schedule
1	**Number Systems and Codes** Decimal, Binary, Octal, and Hexa-decimal number systems and their conversions.	CO1	1) Convert $(75.56)_{10}$ to binary format. 2) Convert $(AB.DD)_{16}$ to Octal format.	Lecture/ Discussion	Assignment-I /Quiz- I
2	Binary arithmetic, Complement representation of negative numbers.	CO1	1)Represent +25 and -25 in 1's complement form and 2's complement form. 2)Add the following binary numbers $(1101)_2 + (1000)_2$.	Lecture/ Discussion	Assignment-I /Quiz- I
3	Subtraction using 1's,2's,9's and 10's complement.	CO1	1) Subtract $(1001)_2 - (1000)_2$ using 2's complement method. 2) Subtract $(45)_{10} - (55)_{10}$ using 9's complement method.	Lecture/ Discussion	Assignment-I /Quiz- I
4	ASCII code, Excess-3 code, Gray code, Error detection and correction, Parity generators and checkers.	CO1	1) Generate the 7 bit even parity hamming code for the message 1000. 2) Convert $(101010)_2$ to gray code.	Lecture/ Discussion	Assignment-I /Quiz- I
5	**Boolean Algebra and Logic gates** Fundamental postulates of Boolean algebra, Basic theorems and properties, switching functions, Simplification of Boolean equations, Digital logic gates, properties of XOR gates, universal gates.	CO2	1) State and prove De-Morgan's theorem. Simplify the following function using Boolean Algebra X'Z'+Y'Z'+YZ'+XYZ	Lecture/ Design	Assignment-I /Quiz- I
6	NAND/NOR implementations, K-Map-min-terms and max-terms, sum-of- products and product-of-sum representations, Minimization of Boolean functions using Karnaugh map.	CO2	1) How do you convert AOI logic to a)NAND logic and b)NOR logic 2) Mention the properties of XOR gate.	Lecture/ Design	Assignment-I /Quiz- I
7	Don't-care conditions, prime implicants, minimization of functions using Quine-McClusky method.	CO2	1) Minimize the following function using K-Map F(A,B,C,D)=$\sum m(0,1,3,5)$. 2) Minimize the following	Lecture/ Design	Assignment-I /Quiz- I

			function using Tabular Method F(A,B,C,D)= $\sum m(0,1,3,5,7,13,15)$.		
8	**Combinational Circuits** Adders, Subtractor, Multiplexer, Demultiplexer, MUX Realization of switching functions.	CO3	1) Design a full adder using Half Adder. 2) Design a 16x1 Multiplexer using 2x1 Multiplexer.	Lecture/ Design	Assignment-I /Quiz- I
9	MID-TEST-1				
10	Encoder, Decoder, Parity bit generator, Code-converters,	CO3	1) Explain the working of 2x4 decoder. 2) Design a circuit to convert BCD number to Excess-3 Code.	Lecture/ Design	Assignment-II/ Quiz- II
11	Basic PLD's:ROM, PROM, PLA, PAL Realizations.	CO3	1) Implement the following function F(A,B,C)=$\sum m(0,2,4,5,6)$ using PLA logic.	Lecture/ Design	Assignment-II/ Quiz- II
12	**Sequential Circuits and Finite State Machines** Latches: RS latch and JK latch, Flip-flops: RS, JK, D, T flip flops. Race around condition, Master-Slave Flip-flop.	CO4	1) Differentiate between latch and flip-flop. 1) 2) Explain the working of JK Flip-Flop and Explain about Race AroundCondition.	Lecture/ Discussion	Assignment-II/ Quiz- II
13	Excitation Tables, Conversion of flip-flops, Shift registers, Universal Shift register, ripple counters, Synchronous counters, Ring counter, Johnson counter, Up- Down counter.	CO4	1) Convert SR Flip-flop to D Flip-flop. 2) Explain the working of Universal Registers. 3) Design Mod-11 Synchronous Counter using D flip-flop.	Lecture/ Design	Assignment-II/ Quiz- II
14	Analysis and Design of Synchronous Sequential Circuits: Moore and Mealy machine models, State Equations, State Table, State diagram, Synthesis of synchronoussequential circuits-serial binary adder, sequence detector and binary counter.	CO4	1) Differentiate between MooreMachine and Mealy Machine. 2) Design a Sequence detector to detect the sequence 1001 using Mealy Machine.	Lecture/ Design	Assignment-II/ Quiz- II
15	**Digital Logic Families** Introduction to logic families, RTL, DTL, TTL, Schottky TTL and Emitter coupled logic, NMOS, PMOS, CMOS logic.	CO5	1) Explain about TTL open collector NAND Gate with the help of a neat diagram. 2) Realize a PMOS AND-OR-INVERT gate and write its functional table.	Lecture/ Discussion	Assignment-II/ Quiz- II
17	CMOS logic families, Comparison of logic families, CMOS: CMOS Inverter, CMOS characteristics, CMOS/TTL interfacing, Tristate Logic.	CO5	1) Draw the circuit for CMOS NOR Gate and explain its function to realize the logic truth table. 2) Compare the properties of various logic families.	Lecture/ Discussion	Assignment-II/ Quiz- II
18	MID-TEST-2				
19/20	END EXAM				