# DIGITAL LOGIC DESIGN

**Course Code:** 22EC1103

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**Course Outcomes:** At the end of the course the student will be able to

CO1: Discuss the significance of number systems, conversions, binary codes. (L2)
CO2: Apply different simplification methods for minimizing Boolean functions. (L3)
CO3: Analyze the design concepts of various combinational circuits.(L4)
CO4: Analyze the concepts of sequential logic design.(L4)
CO5: Categorize Mealy & Moore models and Design Synchronous Sequential machines.(L4)

## UNIT-I 10 Lectures

**Number Systems and Codes**

Decimal, Binary, Octal, and Hexa-decimal number systems and their conversions, BCD Code, Excess-3 code, Gray code, Error detection and correction- Parity, Hamming code, Complement representation of negative numbers.

Verilog codes of 1's complement and 2's complement arithmetic, BCD addition and Parity generator in Dataflow level modelling.

Learning outcomes: At the end of this unit, the student will be able to

1. understand the advantages of using different number systems (L2)
2. describe different binary codes (L2)
3. summarize error detection and correction concepts (L2)

## UNIT-II 8 Lectures

**Boolean Algebra & Logic Gates**

Boolean operations, Boolean functions, algebraic manipulations, min-terms and max-terms, sum- of-products and product-of-sum representations, logic gates, NAND/NOR implementations, Minimization of Boolean functions using K - map, don't-care conditions, prime implicants.

Gate level Verilog codes of SOP and POS expressions using basic gates and universal gate primitives.

Learning outcomes: At the end of this unit, the student will be able to

1. apply basic laws & De Morgan's theorems to simplify Boolean expressions(L3)
2. understand the concepts of sum-of-products and product-of-sums representations (L2)
3. describe K- Map method of minimizing logic functions (L2)

## UNIT-III 12 Lectures

**Combinational Circuits**

Analysis of combinational circuits, Design Procedure Binary Adder, subtractor, comparator, decoders, encoders, multiplexers, demultiplexers, Code Converters. Parity generator and checker, Basic PLD's - ROM, PROM, PLA, PAL Realizations.

Verilog codes of half adder, full adder, 2 to 4 decoder, code converters in Gate level modelling.

Verilog codes of 2:1 multiplexer, 1:4 demultiplexer in Behavioral level modelling.

Learning outcomes: At the end of this unit, the student will be able to
1. outline the concepts of combinational digital circuits (L4)
2. describe combinational circuits such as adders, subtractors, multipliers, comparators (L2)
3. analyze the digital circuit design using PLDs (L4)

**UNIT-IV** **10 Lectures**

**Sequential Circuits**

Latches: RS latch and JK latch, Flip-flops: RS, JK, D, T flip flops, Master-slave flip flops, Edge- triggered flip-flops. Shift registers, ripple counters, synchronous counters, Ring counter, Johnson counter, Up-Down counter.

Verilog codes of Flip-Flops, 4-bit shift register in Behavioral level modelling.

Learning outcomes: At the end of this unit, the student will be able to
1. understand behaviour of Flip-Flops and Latches (L2)
2. summarize the concepts of Shift Registers (L2)
3. analyze the design of Counters (L4)

**UNIT-V** **10 Lectures**

**Finite State Machines**

Analysis and Design of Synchronous Sequential Circuits: Moore and Mealy machine models, State Equations, State Table, State diagram, State reduction & assignment, Synthesis of synchronous sequential circuits- serial binary adder, sequence detector, and binary counter, Partition technique for completely specified sequential machines.

Learning outcomes: At the end of this unit, the student will be able to
1. understand Moore and Mealy machine models (L2)
2. discuss the concepts of state assignment and state reduction (L2)
3. analyze the design and synthesis of synchronous sequential circuits (L4)

**Text Books:**

1. M. Morris Mano and Michael D. Ciletti, *Digital Design*, 4th Edition, Pearson Education, 2013.
2. T.R. Padmanabhan and B. Bala Tripura Sundari, *Design through Verilog HDL*, WSE, IEEE Press. 2004.

**References:**

1. A. Anand Kumar, *Switching Theory and Logic Design*, PHI, 2014.
2. Z. Kohavi, *Switching and Finite Automata Theory*, 2nd Edition, Tata McGraw Hill, 2008.
3. Charles H Roth (Jr), Larry L. Kinney, *Fundamentals of Logic Design*, 5th Edition, Cengage Learning India Edition, 2010.
4. John.M Yarbrough, *Digital Logic Applications and Design*, Thomson Learning, 2006.