DIGITAL DESIGN THROUGH VERILOG
(Elective-III)

Course Code:13EC1132

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Pre requisites: Switching Theory and Logic Design.

Course Educational Objectives:

To learn the concepts of modeling a digital system using Verilog hardware description Language.

Course Outcomes:

- Students can model digital circuits using Verilog.
- Student can represent Function of any digital system using hardware description language

UNIT-I **(10 Lectures)**

INTRODUCTION TO VERILOG:

Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches.

LANGUAGE CONSTRUCTS AND CONVENTIONS:

Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks.

UNIT-II **(14 Lectures)**

GATE LEVEL MODELING:

Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flipflops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits.

DATA FLOW LEVEL MODELING:

Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators.

UNIT-III (14 Lectures)

BEHAVIORAL MODELING:

Introduction, Operations and Assignments, Functional Bifurcation, *Initial* Construct, *Always* Construct, Examples, Assignments with Delays, *Wait* construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-blocking Assignments, The case statement, Simulation Flow. i*f* and i*f*-else constructs, assign-deassign construct, repeat construct, for loop, the disable construct, whileloop, forever loop, parallel blocks, force-release construct, Event.

SWITCH LEVEL MODELING:

Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Tri-reg Nets.

UNIT-IV (12 Lectures)

FUNCTIONS, TASKS, AND U SER-DEFINED PRIMITIVES:

Introduction, Function, Tasks, User- Defined Primitives (UDP), FSM Design (Moore and Mealy Machines).

SYSTEM TASKS, FUNCTIONS AND COMPILER DIRECTIVES:

Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations.

VERILOG MODELS FOR MEMORIES AND BUSES:

Static RAM Memory, A simplified 486 Bus Model, UART Design.

UNIT-V (10 Lectures)

DESIGNING WITH FIELD PROGRAMMABLE GATE ARRAYS AND COMPLEX PROGRAMMABLE LOGIC DEVICES:

Xilinx 3000 Series FPGAs, Designing with FPGAs, Using a One-Hot State Assignment, Altera Complex Programmable Logic Devices (CPLDs), Altera FLEX 10K Series CPLDs.

TEXT BOOKS:

1. T.R. Padmanabhan and B. Bala Tripura Sundari, "*Design through Verilog HDL",* WSE, IEEE Press 2008.
2. J. Bhaskar, *"A Verilog Primer"*, BSP, 2nd edition 2003.

REFERENCES:

1. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition,2003.
2. Thomas and Moorby, *"The Verilog Hardware Description Language"*, kluwer academic publishers, 5th edition, 2002.
3. Stephen Brown and Zvonko Vranesic, *"Fundamentals of Logic Design with Verilog"*, TMH publications, 2007.
4. Charles.H.Roth,Jr., Lizy Kurian John *"Digital System Design using VHDL"* , Thomson, 2nd Edition, 2008