VLSI DESIGN

(Common to ECE and EEE)

Course Code: 13EC1117

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Pre requisites: Electronics Devices and Circuits, Switching Theory and Logic Design.

Course Outcomes:

At the end of the course the student will be able to

CO 1 Distinguish different IC technologies and basic electrical properties of MOS, CMOS and Bi-CMOS circuits.

CO 2 Draw stick diagrams, layout diagrams for logic gates and understand different scaling models.

CO 3 Design subsystem consisting of Combinational and sequential circuits

CO 4 Comprehend CPLD, FPGA architecture and standard cells.

CO 5 Comprehend tools for design and verification.

UNIT-I **(15 Lectures)**

INTRODUCTION TO MOS TECHNOLOGIES:

VLSI Design Flow, Introduction to IC Technology–MOS, PMOS, NMOS, CMOS & Bi-CMOS technologies.

BASIC ELECTRICAL PROPERTIES:

Basic Electrical Properties of MOS and Bi-CMOS Circuits: I_{ds}-V_{ds} relationships, MOS transistor threshold Voltage, g_m, g_{ds}, figure of merit, Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design, Bi-CMOS Inverters.

UNIT-II (12 Lectures)

VLSI CIRCUIT DESIGN PROCESSES:

MOS Layers, Stick Diagrams, Design Rules and Layout, CMOS Design rules for wires, Contacts and Transistors, Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits, Limitations of Scaling.

UNIT-III (14 Lectures)

GATE LEVEL DESIGN:

Transmission Gates, Alternate gate circuits, Basic circuit concepts: Sheet Resistance R_S and its concept to MOS, Area Capacitance Units, Calculations, Delays, Driving large Capacitive Loads, Wiring Capacitances, Fan-in and fan-out, Choice of layers.

SUBSYSTEM DESIGN:

Shifters, Adders, ALUs, Multipliers, Parity generators, Comparators, Zero/One Detectors, High Density Memory Elements.

UNIT-IV (9 Lectures)

SEMICONDUCTOR INTEGRATED CIRCUIT DESIGN:

FPGAs (Xilinx 4000series), CPLDs (Xilinx 9500series), Standard Cells, Design Approach.

UNIT-V (10 Lectures)

DESIGN METHODS AND TESTING:

Design methods, Design capture tools, Design Verification Tools, CMOS Testing, Need for testing, Test Principles, Design Strategies for test, Chip level Test Techniques, System-level Test Techniques, Layout Design for Improved Testability.

TEXT BOOKS:

1. Kamran Eshraghian, Eshraghian Dougles and A.Pucknell, *"Essentials of VLSI circuits and systems"*, 3rd Edn, PHI, 2005.
2. Weste and Eshraghian, *"Principles of CMOS VLSI Design"*, Pearson Education, 3rd edn 1999.

REFERENCES:

1. John .P. Uyemura, *"Introduction to VLSI Circuits and Systems"*, John Wiley, 1st Edition. 2009.
2. Sabastian smith, *"Application Specific Integrated Circuits"*, Addison Wesley Publishing Company Incorporated, 2008
3 John F.Wakerly, *"Digital Design Principles & Practices"*, PHI/ Pearson Education Asia, 3rd Edition, 2005.
4. John M. Rabaey, *"Digital Integrated Circuits"*, PHI, EEE, 2*nd* Edition 2003.
5. Wayne Wolf, *"Modern VLSI Design"*, Pearson Education, 3rd Edition, 2008.
6. Behzad Razavi, *"Design of Analog CMOS Integrated Circuits"*, The McGraw Hill, 2001.